Sensors and Actuators A 279 (2018) 284–292

Contents lists available at ScienceDirect

Sensors and Actuators A: Physical

journal homepage: www.elsevier.com/locate/sna

# An ASIC chip with pipeline ADCs for CCD sensor imaging system

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ARTICLE INFO

*Article history:*
Received 12 November 2017
Received in revised form 14 May 2018
Accepted 6 June 2018
Available online 19 June 2018

*Keywords:*
ASIC
ADC
Photoelectric sensor
CDS
CCD
Image

ABSTRACT

This paper introduces the design of an application specific integrated circuit (ASIC). It will conduct the image processing for photoelectric image sensor charge coupled device (CCD). The ASIC can convert the analog signal of CCD into a suitable digital signal, which is used as the input for the next stage. To realize the ASIC, a two-channel analog to digital converter (ADC) with the speed of 40 MS/s-100 MS/s and a low voltage differential signaling (LVDS) has been proposed. In the ASIC, the correlated double sampling (CDS) has been integrated into the programmable gain amplifier (PGA). A novel CDS circuit is employed to reduce the amplifier gain error. The unique design reduces the size of ASIC by sharing the same operational amplifier (OPA) block. In the low sampling rate of 40 MHz, the spurious-free dynamic range (SFDR) is larger than 91 dB, and the signal-to-noise-ratio (SNR) is more than 79 dB. In the high sampling rate of 100 MHz, the ADC achieved a high SFDR of 92.2 dB and SNR of 81.47 dB. With a 0.13-μm 1P-6M CMOS process, the ASIC only occupies on the die with a size of 21.16 $mm^2$. With the power supply of 3.3 V and 1.8 V, the power consumption is as low as 405 mW. By using the ASIC with the specially designed ADC, the saturated output image reaches a high SNR of 52.2 dB.



## 1. Introduction

CCD is a kind of photoelectric image sensor, which can convert optical signals into electrical signals [1]. With the advantages of high light quality, small volume, low power consumption, large dynamic range, high-precision, and long service time, CCD has been widely used in space remote sensing observation system, earth observation and other fields [2].

The time delay integral (TDI) CCD is a type of plane array image sensor, which is used in line-scan mode. It can repeatedly capture the same scene image, increasing the responsiveness of targets. Recently, spatial optical remote sensing imaging technology with low power consumption and high precision has been paid more and more attention. The traditional design method has not achieved [3–5]. For some particular application requirements, we can integrate with some special circuits to achieve. This type of imaging processing circuit emphasizes high dynamic range and low SNR performance.

In this paper, we integrate two specific circuits to conduct the image processing for photoelectric sensors. The first one is based on the ADC, which increases the correlated double sampling circuit. The second one is based on a serial LVDS, which exports digital signals. Both circuits are fully integrated to form an image processing circuit. The circuit should be able to convert the analog signals of CCD to the most proper serial LVDS digital signals. This way, digital signals can be quickly received by the back-end. The ADC part is the most challenging circuit so that this paper will mostly introduce the ADC circuit [6]. Among various ADC architectures, the pipeline ADC is widely used in Nyquist-sampling applications. The pipeline ADC cannot only achieve high-resolution but also has a high throughput. This work describes the design of a 14-b pipeline ADC with 100 MS/s in a 0.13-μm CMOS process.

The following section of this paper introduces the TDI CCD image system and discusses the challenges of the system. Section 3 presents the analysis and design of a specific integrated circuit. Section 4 presents and discusses experimental results of the circuit itself and the imaging system by using the circuit. Finally, conclusions are given in Section 5.

## 2. Image system

### 2.1. TDI CCD structure and theory

TDI CCD image detector is a type of plane array structure sensor with line-scan output mode. It has the function of doing multiple

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https://doi.org/10.1016/j.sna.2018.06.014
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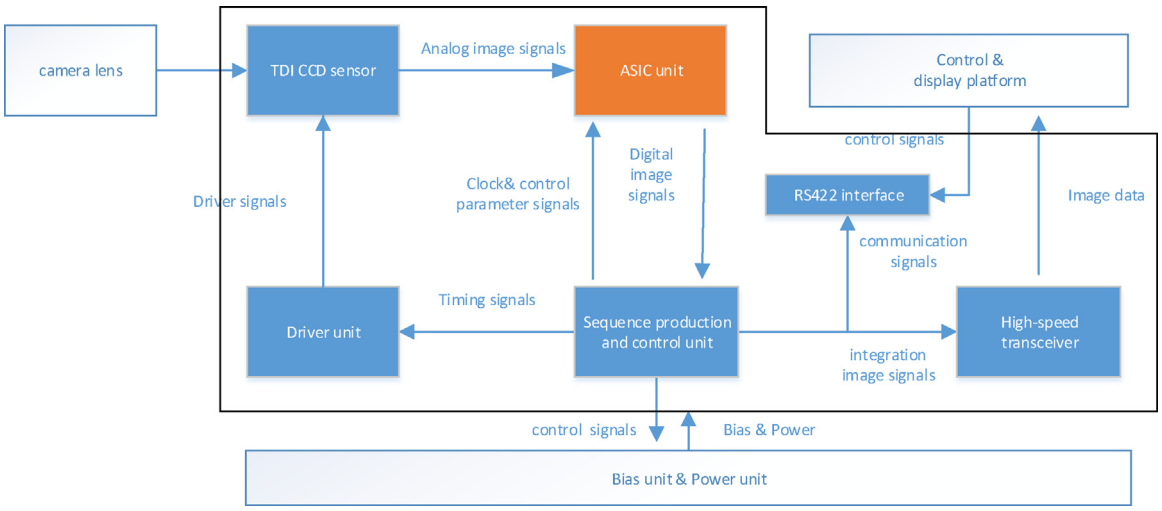



**Fig. 1.** TDI CCD image system block diagram.

series of time-delayed integral. There are four spectral zones in TDI CCD image sensor. One is panchromatic spectral zone, and others are multi-spectral zones. There are 96 lines of pixels in the panchromatic spectral zone and 6144 pixels in each line. That means the panchromatic spectral zone has 96 stages of time delay integration. The charges of the sensor are along the direction of the stages to accumulate electric charge. Integral series from Level 1 to level 96 is ordered from the bottom up. With the movement of remote sensing camera, the integral series from level 96 to level 1will be exposed imaging in turn. Charges accumulate from level 96 to level 1 step-by-step to form charge packet. Finally, the charge packet transforms into the shift output register of the TDI CCD image sensor. At the moment, the amplitude of output signal is the accumulated value of 96-pixel charges, just like that a pixel generates the charge quantity of 96 times integration period. The amplitude of output signals increase by 96 times, but the noise only increases to $96^{1/2}$ times. Thus, the SNR of M stages integral series TDI CCD image sensor was improved by $M^{1/2}$ times compared to the conventional linear CCD image sensors.

### 2.2. TDI CCD image system

A high-speed multispectral TDI CCD sensor focal plane imaging system is shown in Fig.1. The system mainly includes multispectral TDI CCD sensor, drive unit, a bias unit, power unit, ASIC unit, sequence unit, control unit, and interface unit. The primary purpose of ASIC unit is to convert the analog signals from the output of the sensor to appropriate digital signals.

TDI CCD sensor converts the optical signals to the analog voltage signals [7–9]. The drive unit produces many drive signals to ensure that the sensor can work in normal condition. Bias unit and power unit supply the suitable voltages to the sensor. The ASIC unit is used to process sensor analog signals by the CDS, dark level correction, and ADC. The sequence production and control unit is used to produce the correct work timing signals for the TDI CCD sensor, merge and package the image data [10,11]. The RS422 interface unit communicates with a control platform. The high-speed transceiver changes parallel digital image data into serial LVDS imaged data and sends it to the display platform.

At the same time, the control and display platform receives image data from the high-speed transceiver. It is also communicating with the imaging system by the RS422 interface unit. The imaging system uses the FPGA as the control core. The system needs to receive and process multi-channel high-speed image data and send high-frequency parallel image data to the transceiver. The Xilinx XC5 VLX50 T is utilized as the processor, which has high-speed processing capability and enough I/O resources. The imaging system is based on the principle of the time-division multiplex to complete disposing and merging multi-channels image data onto the FPGA. The high-speed transceivers recompose the merged image data and encode into high-speed serialization LVDS image data, which sent to the imaging equipment for display.

## 3. ASIC ANALYSIS and DESIGNING

### 3.1. ASIC diagram

The ASIC chip block diagram is shown in Fig.2. The ASIC chip mainly consists of CDS circuit, PGA circuit, 14-bit pipeline ADC circuit, LVDS output circuit and other peripheral circuits. There are three steps for ASIC chips processing the analog image signals from the CCD sensor. Firstly, the CDS circuit receives analog image signals. Secondly, the PGA and pipeline ADC circuit convert analog signals into parallel digital signals. Finally, the LVDS output circuit encodes parallel digital signals into LVDS signals. Since the pipeline ADC is the critical part of the system, the following will mostly introduce the pipeline ADC [12].

The signal to noise plus distortion ratio (SNDR) and the sampling rate of an ASIC can be calculated from the specifications of the sensor. The maximum measured value of saturation full well capacity for the sensor is around 400 ke-. With a 10 dB margin, the minimum dynamic range needs to be larger than 70 dB. According to the 6 dB/bit theory, the effective number of bits (ENOB) of ADC needs to be more than 11-bit. Finally, 14-bit is chosen for practical system applications. The maximum speed of pixel transmission is 19 MHz. So the minimum required sampling rate need to be above 38 MHz.

### 3.2. Pipeline ADC theory

The structure of the pipeline ADC is based on multistage amplitude comparator. The digitization is performed by many steps with a cascade of several similar stages of limited resolution ADC. Each stage samples the output signal of the last stage and holds it to the next stage by a sample-hold circuit. The pipeline ADC enables high conversion throughput with non-overlapping clocks. A typical pipeline stage is illustrated in Fig.3. The signal passed to the next stage is the conversion result of the current stage created by a digital to analog converter (DAC) and a subtraction circuit.

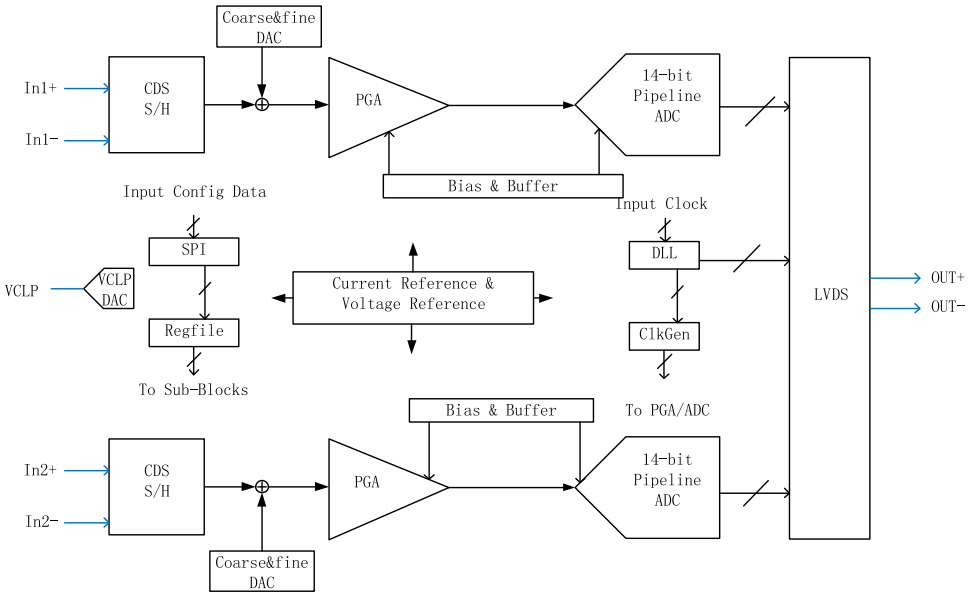



**Fig. 2.** The ASIC block diagram.

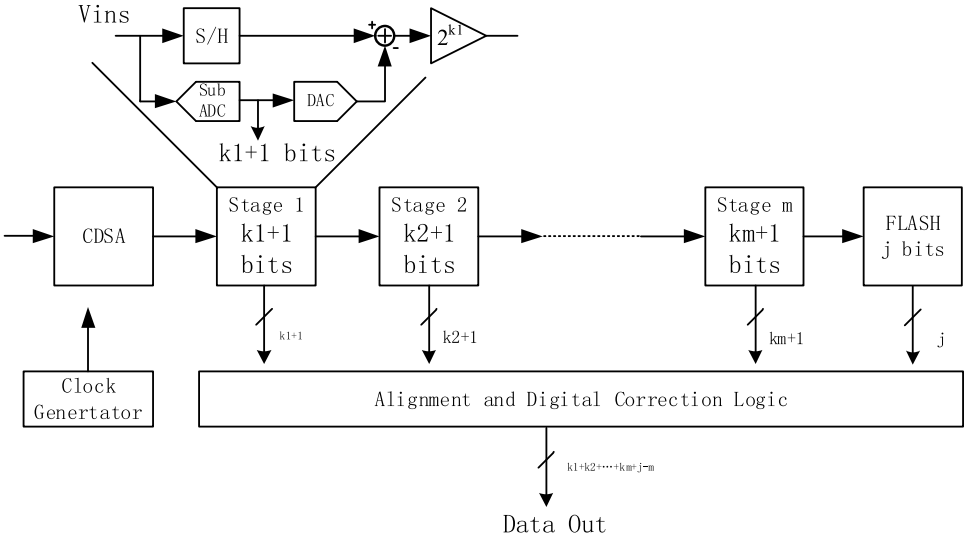



**Fig. 3.** The pipeline ADC block diagram.

The input signal of every stage is quantized as the digital signal by a sub-ADC, and the result is output as a quantization result of this stage. At the same time, a DAC converts the digital signal into the analog sigsult is output as a quantization result of this stage. At the same time, a DAC converts the digital signal into the analog signals, which are subtracted from the input signal. The result was amplified by $2^{k1}$ times as the input for the next stage of the pipeline ADC.

The number of comparators has a linear relationship of the bits of sub-ADC in the pipeline ADC. Therefore, the number of comparators is greatly reduced. In this paper, there are seven stages in the whole ADC. The last stage is a 2-bit flash ADC. Others are all sub-ADCs. Each sub-ADC is 3-bit. The power consumption and the area of the circuit are primarily reduced by using digital calibration algorithm. For medium to high-resolution and high conversion rates, pipeline ADCs have been demonstrated to achieve the lowest power consumption [13–17].

### 3.3. Analysis of the non-ideal factors

A pipeline stage is mainly composed of comparators and MDAC, which includes sub-ADC, sample-hold circuit and an amplifier. Therefore, the error of a pipeline ADC is composed of these sub-module errors. The main non-ideal factors of the MDAC include capacitor mismatch, amplifier disorders, finite gain, finite bandwidth, finite output resistance, the input port parasitic capacitor and clock jitter. Moreover, the error of the comparator mainly comes from capacitor mismatch which can lead to the decision level drift of the sub-ADC. So that, it affects the final digital output codes. The disorder of the comparator mainly comes from the mismatch of the MOS tube. The fluctuation of the reference voltage can be equal to the input fluctuation of the comparator.

#### 3.3.1. Capacitor mismatch error

For the switching capacitor circuit of the MDAC, the matching accuracy between capacitors is an important parameter that deter-

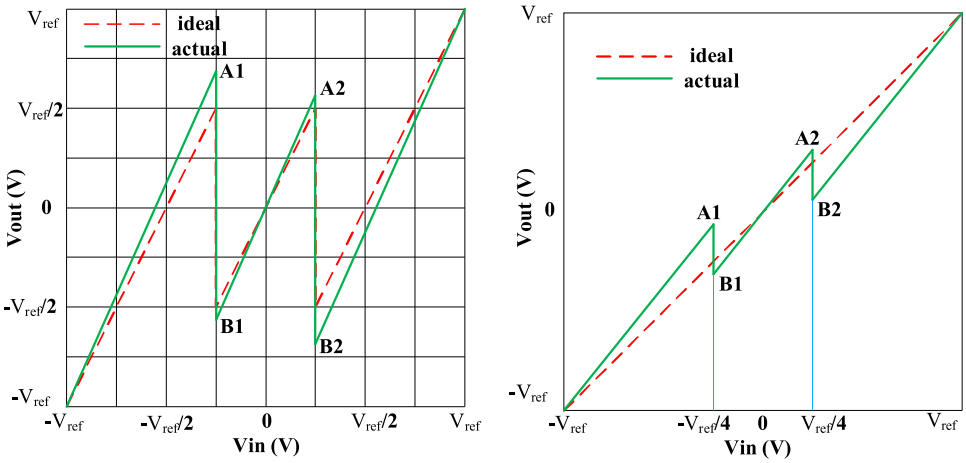



**Fig. 4.** 1.5-bit transfer function with capacitor mismatch error.

mines the multiple of the residual gain amplification. It is critical to the SFDR. For MDAC, if capacitors are ideal and no other non-ideal factors are considered, the output voltage of the MDAC can be expressed as

$$V_{out,i} = V_{in,i}C_f + \sum_{j=1}^{n-1} C_{s,j}/C_f - V_{ref}\sum_{j=0}^{n-1}(m_j C_{s,j})/C_f \tag{1}$$

Where $C_f$ is feedback capacitor, $C_s$ is sampling capacitor. According to the output result of comparators that $m_j$ can take one number from {-1,0,1}. $V_{in,i}$ is the input voltage. $V_{ref}$ is the reference voltage.

Taking into account the capacitor mismatch error, We rewrite the results as

$$V_{out,i} = \frac{C_f + \Delta C_f + \sum_{j=1}^{n-1}(C_{s,j} + \Delta C_{s,j})}{C_f + \Delta C_f} V_{in,i} - \frac{\sum_{j=0}^{n-1}(m_j(C_{s,j} + \Delta C_{s,j}))}{C_f + \Delta C_f} V_{ref} \tag{2}$$

The first half part of (2) represents the gain error caused by the capacitor mismatch error. The latter half part of (2) represents the capacitor mismatch error which is equivalent to the error introduced by the decision level drift of the comparators.

If $C_f$ is equal to $C_s$ and is equal to C, the total capacitor error can be expressed as

$$\alpha = \sum_{j=0}^{n-1} \frac{\Delta C_{s,j} - \Delta C_f}{C + \Delta C_f} \tag{3}$$

It is only considering the effect of the capacitor mismatch error. The actual curve will deviate from the ideal curve at each turning point. The margin transferred function curves, with 1.5-bit as an example, are shown in Fig. 4.

As the MDAC gain becomes larger, the above two points A1 and A2 of the two corners in Fig.4 are larger than the ideal value. The following two points B1 and B2 are smaller than the ideal value. It will cause the transfer function curve of the whole ADC to be nonlinear. To ensure the linearity of the ADC, we should let the capacitance mismatch error meet the requirements of the next pipeline stage. In practice, we can only achieve an accuracy of less than 12-bit ADC by the capacitor matching [18].

Since the output impedance of the OPA is unlikely infinite, the open-loop gain is limited. The feedback coefficient of the OPA is smaller if the parasitic capacitor of the input is taken into account. Based on the above non-ideal factors, the output expression of MDAC is rewritten, and the effect of capacitor mismatch error is neglected to simplify the analysis.

$$V_{out,i} = \left( \frac{C_f + \sum_{j=0}^{n-1} C_{s,j}}{C_f} V_{in,i} - \frac{\sum_{j=0}^{n-1} m_j C_{s,j}}{C_f} V_{ref} \right) \frac{1}{1 + \frac{1}{A_0 f}} \tag{4}$$

The effect of the finite gain is to reduce the slope of the transfer function curve of the MDAC, which is the reciprocal of the loop gain of the OPA. The OPA direct current (DC) gain determines the static error of the MDAC. If the residual resolution is N, then the error allowed of the current stage has to be within 1/2N + 1. Assuming half of the total error is due to static error, and then the static error must be less than 1/2N + 2. If $A_0 f$ is much bigger than 1, the static error can be expressed as

$$\varepsilon_{static} = \frac{1}{A_0 f} < \frac{1}{2^{N+2}} \tag{5}$$

So the OPA gain needs above $2^{N+2}/f$.

### 3.3.2. Slew rate and bandwidth

The OPA gain is not enough to affect the static performance of ADC. The finite slew rate and bandwidth affect the dynamic performance. Both determine OPA output build speed and accuracy in a finite time. The settling accuracy of OPA determines the dynamic error of MDAC which must be less than 1/2N + 2 if the static error is also 1/2N + 2.

The operating cycle consists of $T_{sr}$ and $T_{se}$. $T_{sr}$ is the time limited by the slew rate of the holding phase, $T_{se}$ is the exponential establishment time. In the worst case, OPA's output capacitor and the sampling capacitor of next stage are both OPA's load. The output of OPA and the slew rate is linear during slewing process. The output voltage during linear settling can be written as

$$V_{out,i}(t) = V_{out,i}(t = \infty)(1 - e^{-\frac{g_m}{C_{L,H}} ft}) \tag{6}$$

where $C_{L,H}$ is the effective load of the MDAC in the holding phase, and f is operating frequency.

The dynamic error can be derived as

$$\varepsilon_{dynamic} = e^{-\frac{g_m}{C_{L,H}} f T_{se}} < \frac{1}{2^{N+2}} \tag{7}$$

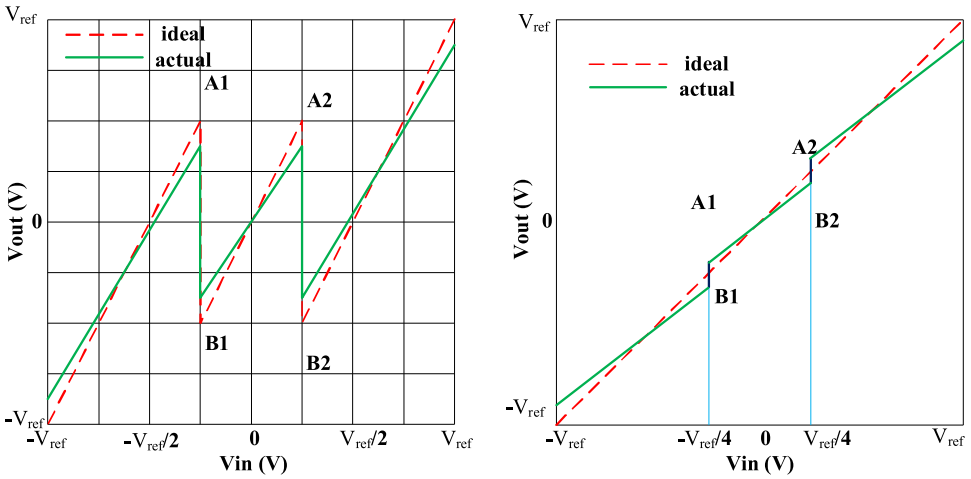



**Fig. 5.** 1.5-bit transfer function with OPA gain error.

The above description shows that the exponential settling process is related to time, so the error is related to signal. We can only reduce this error by increasing the OPA bandwidth or the settling time. It is difficult to eliminate it with other error elimination or correction methods. The impact on the establishment of the ADC accuracy will reduce the SNR, which will reduce the performance of the ADC. In general, slewing process takes about one-fourth to one-third of the total settling time, which is approximately 1 ns. The linear settling spends 2 ns or 3 ns [19,20]. The margin transferred function curves to take 1.5-bit as an example, as shown in Fig.5. It is only considering the effect of OPA gain error and finite settling error. Because of the finite gain and settling time of the OPA, the slope of the actual transfer function curve is smaller than the ideal value. The two points A1 and A2 of the two corners in Fig.5 are smaller than the ideal value. The following two points B1 and B2 of the two corners are larger than the ideal value.

### 3.3.3. *Clock jitter*

The MDAC with switch capacitor architecture requires the clock to control the switch on and off. The actual clock has clock jitter, and the rising and falling edges of the clock signal also take up some time, so the clock determines the performance of the circuit. The sampling switch clock is the most important of these clocks. The input signal is associated with time. The clock jitter of the sampling clock will cause the sampling of the signal to be erroneous making the SNR worse. The circuit design cannot eliminate the impact of the clock jitter. It only makes the impact on the clock jitter as small as possible, until the impact on circuit performance is negligible [21]. The input clock circuit is a differential low-noise buffer. To minimize the sources of clock jitter, we employ P-substrate contacts and deep N-well isolation to eliminate crosstalk. The clock signal was also carefully shielded by ground.

### 3.4. *Correlated double sampling topology structure*

It essentially to resolve the problems that the OPA's finite gain leads to the sampling error in sampling schematics. Previously, several techniques have been developed to solve the problems result in much more power dissipation, such as several stage amplifiers, gain-boost circuits. For this design, a correlated double sampling topology structure is illustrated with Fig.6, which can acquire very low error of output signal with low cost. At the same time, the output analog signal of CCD needs to use CDS technique achieving sampling [22,23].

The solid part of Fig.6 is the traditional S/H (sample/hold) topology, and the dotted line adds a supplementary way to achieve the

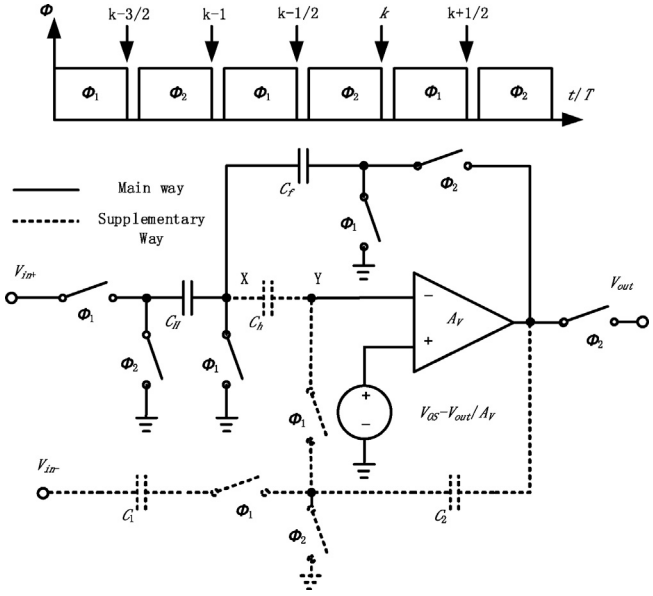
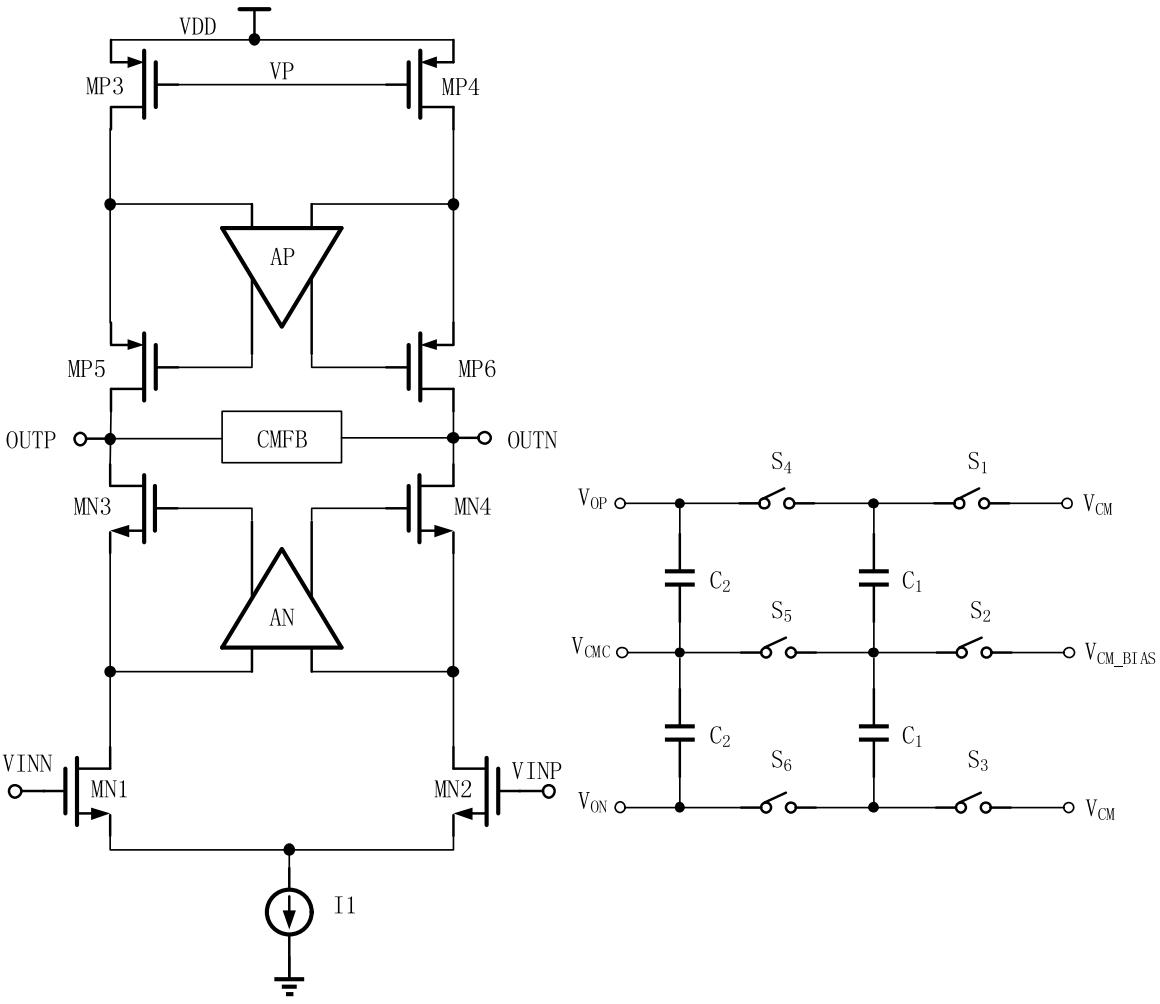



**Fig. 6.** CDS topology structure.

CDS technique. Compared with the traditional S/H circuit, the correlated double sampling technique can eliminate the amplifier offset VOS and reduce voltage effect of output feedback brought by the limited gain Av at the same time, so as to improve the accuracy of the system.

$\Phi_1$ and $\Phi_2$ are two non-overlapping clock signals. When $\Phi_1$ is valid, the main way is separated from the amplifier and the capacitor $C_H$ samples the input signal $V_{in+}$ on the left side. The supplementary way and the amplifier compose an integrator to make the output signal tracking the input signal. The capacitor $C_h$ stores $V_{OS}$ and $-V_{out}/A_V$ on the right side. When $\Phi_2$ is valid, the main way is separated from the amplifier and the capacitor $C_H$ samples the input signal $V_{in+}$ on the left side. The supplementary way and the amplifier compose an integrator to make the output signal tracking the input signal. The capacitor $C_h$ stores $V_{OS}$ and $-V_{out}/A_V$ on the right side. The supplementary way is disconnected, and the main way achieves holding and amplification. The node X is no longer affected by $V_{OS}$ due to the effect of capacitor $C_h$. According to the law of conservation of charge, the gain error of the CDS circuit is reduced by $(1+C_1/C_2)/A_V^2$ times.




(a) the first stage CMOS gain-boosting amplifier (b) SC-CMFB circuit of gain-boosting amplifier

**Fig. 7.** (a) The first stage CMOS gain-boosting amplifier (b) SC-CMFB circuit of the gain-boosting amplifier.

### 3.5. *The amplifier of the first stage*

The amplifier is an essential part of high-speed and high-resolution pipeline ADC. It determines the speed and resolution of the ADC and occupies the main power consumption and area. The first stage pipeline ADC is the best important in all stages. Delivering sufficient DC gain on low power dissipation is a difficult challenge to OPA design at a high sampling rate. Although a multi-stage structure offers high DC gain, the circuit needs more power for the necessity of frequency compensation. Single-stage architectures can offer large GBW (gain bandwidth) with limited DC gain due to the low output resistance. This paper presents a tradition CMOS gain-boosting technique amplifier in Fig.7(a). The boosting amplifiers all use a folded-cascode structure OPA. SC-CMFB (Switch Capacitor Common mode feedback) circuit is required in fully differential circuits to sense and stabilize the output common mode voltage through the common mode feedback loop. SC-CMFB doesn't affect output swing and consumes no static power. The SC-CMFB circuit is shown in Fig.7(b).

C1 works as a switched capacitor resistor. During holding phase, S1∼S3 are closed, charging the voltage of C1 between VCM signal and VCM_BIAS signal, while C2 is used to sense the output common mode voltage. During resetting phase, S4∼S6 are closed, charging the voltage of C2 between VCM and VCM_BIAS through C1. In general, the size of C2 is designed to be four times to ten times larger than that of C1. Using a too large capacitor for C2 increases the OPA loop load capacitor, while using a too small capacitor for C1 causes common mode offset voltage due to charge injection and clock feedthrough of these switches. This OPA has an excellent result which is above 97 dB with gain and above 0.94 GHz with GBW. The simulation result is shown in Fig.8.

## 4. Measured results and discussion

The ADC was fabricated in a 3.3-V 0.13-μm 1P-6 M CMOS process with metal insulator metal (MIM) structure capacitors and dissipated 405 mW at 100 MS/s. A die photo and his application are shown in Fig. 9. The area of the chip is 4.6 mm*4.6 mm.

Table 1 compares the key performances of this work and others. A 12 bit 53-mW 195 MS/s pipeline ADC is designed using split-ADC calibration. Fully deterministic continuous background calibration was applied to correct for nonlinearity and linear errors in ADC [13]. The research groups have achieved a 100 MS/s, 10.5 bit, 2.46-mW comparator-less pipeline ADC using self-biased ring amplifiers. They are very focused on low power consumption [18]. The authors describe a 14-bit, 125 MS/s IF/RF sampling pipelined ADC that is implemented in a 0.35 m BiCMOS process [21]. Although the BiCMOS process is an old process, it is beneficial to realize high speed and high-resolution ADC. However, the focus of this work is on SNDR, which is very different from Ref. [13], Ref [18]. and Ref

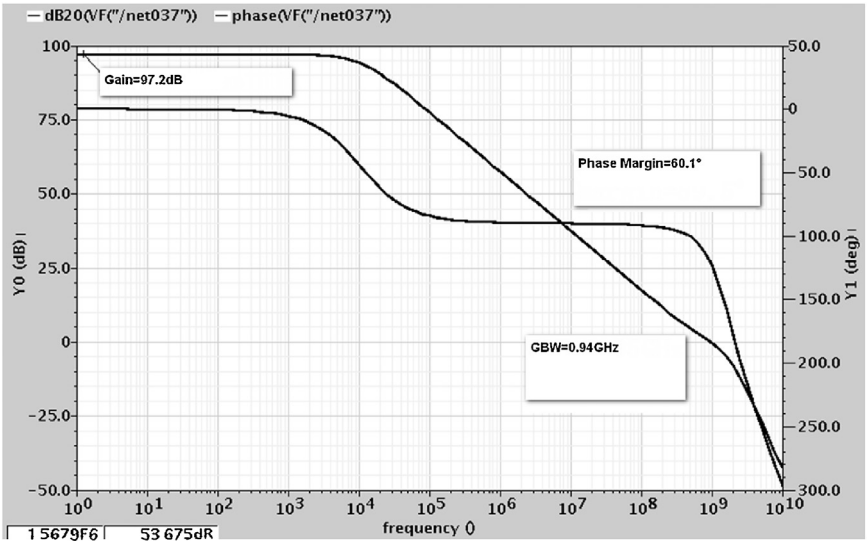



**Fig. 8.** Simulated first stage gain and bandwidth.

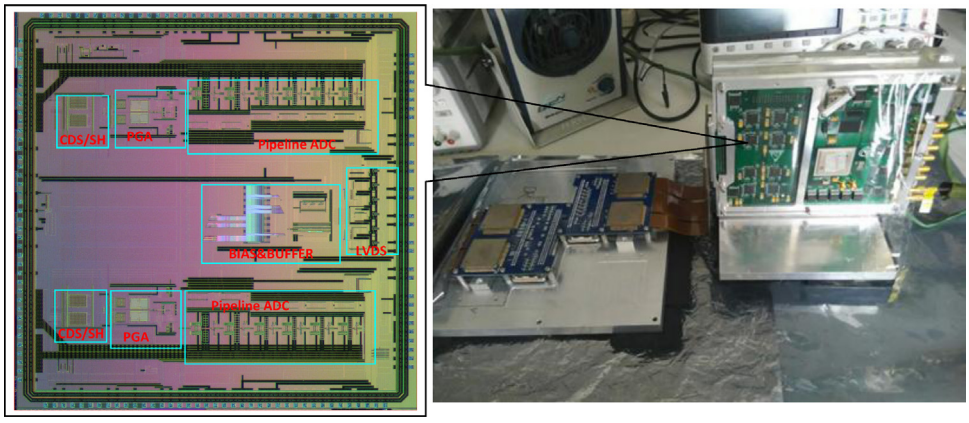



**Fig. 9.** Die photo and application board.

**Table 1**
Performance comparison with other pipeline ADC.

| | This Work | [13] | [18] | [21] |
|---|---|---|---|---|
| Resolution [bits] | 14 | 12 | 10.5 | 14 |
| Fs [MS/s] | 100 | 195 | 100 | 125 |
| Technology | 0.13 μm CMOS | 40 nm CMOS | 65 nm CMOS | 0.35 μm BiCMOS |
| channels | 2 | 1 | 1 | 1 |
| Analog Supply [V] | 3.3 | 1 | 1.2 | 3.3 |
| Active Area [$mm^2$] | 21.16 | 0.81 | 0.097 | 70 |
| \|DNL\| [LSB] | 0.4 | N/A | 0.22 | 0.2 |
| \|INL\| [LSB] | 0.29 | 1.4 | 0.62 | 0.8 |
| SFDR [dB] | 92.7 | 82 | 64.7 | 100 |
| SNDR [dB] | 81.5 | 64.8 | 56.6 | 75 |
| Total Power [mW] | 405 | 53 | 2.46 | 1850 |
| FOM [fj/conv-step] | 369 | 157.5 | 44.5 | 700 |

[21]. work, and this is also the primary contribution of our work. The FOM is 44.5 fj/conv-step in Ref. [18], which is the best result in the Table 1. The SNDR of their work is 56.6 dB. With the difference of the bit number, it is still less than the result of this paper.

The SNR of the imaging system can reflect the merits of the image quality of the image system specifications. The imaging system uses ASIC chips, which is critical to test whether the signal-to-noise ratio can meet the application. Fig.10(d) is the SNR test result of image system which fixes the integrated ball light source brightness and adjusts the system integration time to make the detector from dark to near saturation state. When the system is in the maximum integration time, the detector close to saturation, the SNR can reach 52.6 dB. The number of full-color saturated electrons of the detector are 400 ke-, and the theoretical maximum signal-to-noise ratio is 56.02 dB.

All the measured result is shown in Fig.10. The dynamic linearity of the ADC characterized by analyzing a fast Fourier transform (FFT) from the output codes is shown in Fig.10(a) and (b). The measured output spectrum with an input signal frequency of 20.6 MHz sampled at 100 MS/S is depicted in Fig.10(a). At this frequency,

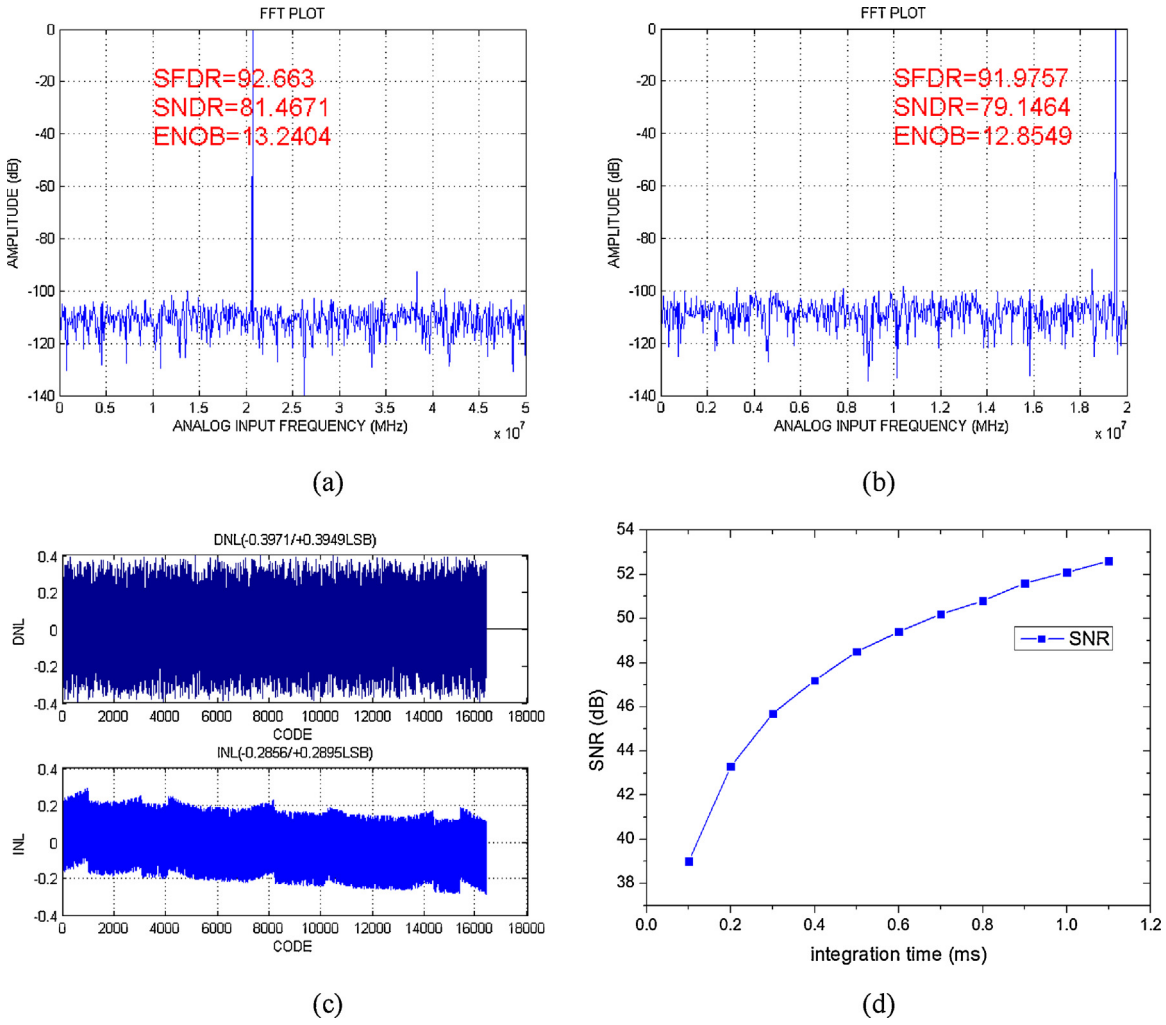



**Fig. 10.** (a) Measured FFT spectrum at fin = 20.6 MHz, Vin = 2 V, fs = 100 MHz and (b) Measured FFT spectrum at fin = 19.5 MHz, Vin = 2 V, fs = 40 MHz (c) Measured DNL and INL (d) measured image system's SNR with integration time.

the measured SFDR and SNDR equal 92.6 dB and 81.5 dB respectively. To measure the input CCD sensor's signal, the ASIC was also tested for an input signal frequency of 19.5 MHz sampled at 40 MS/S. Fig. 10(b) shows the digital spectrum of the ADC output. At this frequency, the measured SFDR and SNDR is 92.0 dB and 79.1 dB respectively. A single pipeline ADC channel dissipates 183 mW. This design results in a figure-of-merit(FOM) of 369 fj/conversion-step for a 20.6 MHz input frequency and a 100 MHz sampling frequency. The differential non-linearity (DNL) and the integral non-linearity (INL) profiles are shown in Fig.10(c). The maximum DNL is 0.4 LSB, and the maximum INL is 0.29 LSB.

The main non-ideal factors include capacitor mismatch, amplifier disorders, finite gain, finite bandwidth, finite output resistance, the input port parasitic capacitor and clock jitter. To reduce the effects of mismatches and asymmetries, we strictly symmetry the circuit design and layout. To reduce the limited gain of the amplifier, we utilize the CDS technology to improve the accuracy of the system. We employ P-substrate contacts and deep N-well isolation to improve clock jitter. A CMOS gain-boosting technique amplifier is used in the first stage. The boosting amplifiers all use a folded-cascode structure op-amp. SC-CMFB circuit is used to sense and stabilize the output common mode voltage through the common mode feedback loop. Since the input amplitude is 2 V, we choice 3.3 V as the analog voltage. And the 0.13-μm process is the minimum size process that supports 3.3 V voltage. The 2 V amplitude can be achieved by 2.5 V analog voltage process, such as 90 nm, 65 nm. But this will increase the power consumption and reduce the reliability.

## 5. Conclusion

This brief describes the design and implementation of an ASIC with binary channels 3.3-V 405-mW 14-bit 10 MS/s ADC in 0.13-μm 1P6M process with MIM capacitors. The ASIC chip, similarly to other signal processing chip, able to convert the photo-electricity sensor signal to digital signal. The test chip demonstrates true 14-b linearity and a 13.24 ENOB in the end. We adopt a novel CDS circuit, which acquires very low error with low cost. Finally, this chip is used in CCD image system which achieves a high SNR system.

The novelty of our development lies in its high SNDR ADC using a CDS circuit. The chip is used in the TDI CCD sensor imaging system. By using the ASIC chip, the imaging system has the advantage of size and SNR. The SNR of this work is much higher than the requirement of the imaging system. In future work, we will focus on low power consumption and small size design with sacrifice SNR. We will also focus on anti-radiation to realize working in space for a long time.

## Acknowledgment

The authors would like to thank all members of photo-electricity sensor detecting team, their contribution and kind support are nec-

essary for this paper. The work is supported by the National Natural Science Foundation of China (No. 41405021).

## References

[1] W.S. Boyle, G.E. Smith, Charge coupled semiconductor devices, Bell Labs Tech. J. 49 (4) (1970) 587–593.
[2] A. Demircan, R. Schuster, M. Radke, et al., Use of a wide angle CCD line camera for BRDF measurements, Infrared Phys. Technol. 41 (1) (2000) 11–19.
[3] D. Wang, W. Li, Y. Yuan, et al., A fine image motion compensation method for the panoramic TDI CCD camera in remote sensing applications, Opt. Commun. 298–299 (298–299) (2013) 79–82.
[4] B.K. Gibson, P. Hickson, Time-delay integration CCD read-out technique: image deformation, Mon. Not. R. Astron. Soc. 258 (3) (1992) 543–551.
[5] B. Wang, J. Bao, S. Wang, et al., Improved line tracing methods for removal of Bad streaks noise in CCD line array image-a case study with GF-1 images, Sensors 17 (4) (2017).
[6] H. Kayahan, M. Yazici, Ö Ceylan, et al., A new digital readout integrated circuit (DROIC) with pixel parallel A/D conversion and reduced quantization noise, Infrared Phys. & Technology 63 (2014) 125–132.
[7] S. Park, H. Uh, S. Choi, A high-sensitivity CCD image sensor using source follower circuit with actively controlled gain characteristics, Sensors & Actuators A Physical 101 (1–2) (2002) 10–13.
[8] M.A. Gottardi, CMOS/CCD image sensor for 2D real time motion estimation, Sensors & Actuators A Physical 46 (1-3) (1995) 251–256.
[9] S. Hamami, L. Fleshel, O. Yadid-Pecht, CMOS image sensor employing 3.3V 12bit 6.3MS/s pipelined ADC, Sensors & Actuators A Physical 135 (1) (2007) 119–125.
[10] Y. Cheng, S. Jin, M. Wang, et al., Image mosaicking approach for a double-camera system in the GaoFen2 optical remote sensing satellite based on the Big virtual camera, Sensors (Basel, Switzerland) 17 (6) (2017).
[11] Y.S. Han, E. Choi, M.G. Kang, Smear removal algorithm using the optical black region for CCD imaging sensors, IEEE Transactions on Consumer Electronics 55 (4) (2009) 2287–2293.
[12] I. Kim, R. Lobo, J. Homer, et al., Sensors. IEEE, Multimodal Analog Front-End for Wearable Bio-Sensors (2015) 1–4.
[13] R. Sehgal, F.V.D. Goes, K. Bult, A 12 b 53 mW 195 MS/s pipeline ADC with 82 dB SFDR using Split-ADC calibration, IEEE J. Solid-State Circuits 50 (7) (2015) 1592–1603.
[14] L. Yong, M.P. Flynn, A 1 mW 71.5 dB SNDR 50 MS/s 13 bit fully differential ring amplifier based SAR-assisted pipeline ADC, IEEE J. Solid-State Circuits 50 (12) (2015) 2901–2911.
[15] J. Lin, D. Paik, S. Lee, et al., An ultra-low-voltage 160 MS/s 7 bit interpolated pipeline ADC using dynamic amplifiers, IEEE J. Solid-State Circuits 50 (6) (2015) 1399–1411.
[16] M. Brandolini, Y.J. Shin, K. Raviprakash, et al., A 5 GS/s 150 mW 10 b SHA-less pipelined/SAR hybrid ADC for direct-sampling systems in 28 nm CMOS, IEEE J. Solid-State Circuits 50 (12) (2015) 2922–2934.
[17] C. Yun, P.R. Gray, B. Nikolic, A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR, IEEE J. Solid-State Circuits 39 (12) (2004) 2139–2151.
[18] L. Yong, M.P.A. Flynn, 100 MS/s, 10.5 Bit, 2.46 mW comparator-less pipeline ADC using self-biased ring amplifiers, IEEE J. Solid-State Circuits 50 (10) (2015) 2331–2341.
[19] E. Sall, A 1.8 v 10-bit 80 MS/s low power track-and-hold circuit in a 0.18 μm CMOS process, IEEE, in: ISCAS'03. Proceedings of the 2003 International Symposium on Circuits and Systems, 2003, 1, 2003, p. I.
[20] Y. Chiu, K. Wojciechowski, A gain-boosted 90-dB dynamic range fast settling OTA with 7.8-mW power consumption, UC Berkeley EE240 Final Proj. Rep. (2000).
[21] A.M.A. Ali, C. Dillon, R. Sneed, et al., A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs jitter, IEEE J. Solid-State Circuits 41 (8) (2006) 1846–1855.
[22] V. Valente, A. Demosthenous, Wideband fully-programmable dual-Mode CMOS analogue front-End for electrical impedance spectroscopy, Sensors 16 (8) (2016) 1159.
[23] M. Ni, F. Li, W. Li, et al., A High-speed analog front-end circuit used in a 12bit 1Gsps pipeline ADC, in: 2015 IEEE 11th International Conference on ASIC (ASICON), IEEE, 2015, pp. 1–4.

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