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Annealing effect on the bipolar resistive switching characteristics of a Ti/Si_3N_4/n-GaN MIS device

Y.R. Chen [a], Z.M. Li [a], Z.W. Zhang [a, *], L.Q. Hu [b], H. Jiang [a], G.Q. Miao [a], H. Song [a, **]

[a] State Key Laboratory of Luminescence and Applications, Changchun Institute of Optics, Fine Mechanics and Physics, Chinese Academy of Sciences, Changchun, 130033, People's Republic of China
[b] College of Physics and Information Engineering, Fuzhou University, Fuzhou, 350002, People's Republic of China

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ABSTRACT

In this paper, the effect of annealing on the bipolar resistive switching characteristics of a Ti/Si_3N_4/n-GaN metal-insulator-semiconductor (MIS) structure memristor is demonstrated. The results show that the stability and repeatability of the bipolar resistive switching are greatly improved in annealed Ti/Si_3N_4/n-GaN MIS devices. The mechanism involved is revealed by both conductive force microscopy (CFM) and x-ray photoelectron spectroscopy (XPS). It is confirmed to *in-situ* local Ti doping in Si_3N_4 by thermal annealing and can be ascribed to the local Ti dopants in the Si_3N_4 bonding the N atoms at positive bias by electro-reductive process that benefits to form stable nanoscale Si filaments. On the contrary, the Si filaments rupture by recombining with N atoms near the n-GaN side at negative bias. The proposed device is apt to integrate with a GaN-based high electron mobility transistor (HEMT) to structure a one-transistor-one-resistor (1T1R) nonvolatile memory cell, which is expected to develop the application of the nitride semiconductors in data storage in addition to the applications in light-emitting diodes, laser diodes, power devices, and photodetectors.

1. Introduction

As a representative of the third generation of semiconductors, nitride semiconductor materials have achieved a great success in optoelectronic and microelectronic applications such as light-emitting diodes (LEDs) [1–3], laser diodes (LDs) [4,5], ultraviolet photodetectors (UV-PDs) [6,7], and high electron mobility transistors (HEMTs) [8,9]. However, there is still lack of memory devices based on nitride semiconductor materials. The research on memory devices based on nitride semiconductor materials is expected to develop their application fields.

In recent years, the nonvolatile memory concept based on resistive switching rather than the traditional charge storage has inspired scientific attention due to its simple architecture, high density integration, and good scalability [10]. The resistive switching, especially, bipolar resistive switching, has been extensively investigated in metal-insulator-metal (MIM) structure with different types of materials as the insulator layer, such as the ferromagnetic materials [11,12], transition metal oxides [13,14], high κ dielectric materials [15,16] and organics [17,18]. Although the sandwich structure of MIM has a lot of advantages such as the simple architecture of the device, the crossbar structure making it easy to realize the memory arrays, and the compatibility with the current micro- and nano-electronic technology fabricated [19], one major issue remains unsolved, viz. the cross-talk occurs both through the insulator and via sneak paths in the nearby cross-points [20]. In addition, the MIM structure is not well suitable for *in-situ* growth of nitride semiconductor materials by metal-organic chemical vapor deposition (MOCVD), because it is difficult to peel off the epitaxial layer from the insulated substrate. The metal-insulator-semiconductor (MIS) structure can be adopted to solve the problems. The development of memristors using nitride semiconductor materials based on MIS structure has the advantages as follows: i) preventing the problem of cross-talk; ii) the possibility to realize monolithic integration with nitride HEMTs to structure one-transistor-one-resistor (1T1R) memory cells (see Fig. S1 in Supplementary Materials).

In our previous work, we have reported on the bipolar resistive switching phenomena in *in-situ* growth of GaN-based materials

* Corresponding author.
** Corresponding author.
E-mail addresses: zhangzw@ciomp.ac.cn (Z.W. Zhang), songh@ciomp.ac.cn (H. Song).

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based on Ni/AlN/n-GaN MIS structure and its mechanism was proved to follow the trap-controlled space charge limited current (SCLC) theory attributing to the nitrogen vacancies of AlN serving as electron traps that formed/ruptured electron transport channel by trapping/detrapping electrons [21]. However, the performances of stability and repeatability are to a large extent limited by the high-density dislocation-related current leakage passages in the AlN material grown by *in-situ* heteroepitaxy [22]. Fortunately, nitride-based dielectric material such as Si_3N_4 is considered to be one of the most promising resistive materials for establishing MIS structure on semiconductors. So far, Si_3N_4-based MIS structure resistive random access memory (RRAM) has been intensively investigated in conventional silicon platform owing to their good compatibility to Si-based CMOS processes, mainly including the Si_3N_4-based single resistive material MIS structure RRAM [23–26], the barrier-embedded bilayer Si_3N_4-based MIS structure RRAM devices with a thin SiO_2 or SiN_x as the barrier layer [27–30], and so on. These research results advantageously prove the effective combination of Si_3N_4 and semiconductors for establishing MIS structure memristors. Herein, we develop a MIS device based on Ti/Si_3N_4/n-GaN and study its resistive switching characteristics for the purpose of obtaining a memristor that can be compatible to the GaN-based HEMTs and realizing a 1T1R nonvolatile memory device based on nitride semiconductor material system. This is expected to develop its application fields. Thus, it is of great significance to develop a highly stable and repeatable Ti/Si_3N_4/n-GaN MIS memory. However, the bipolar resistive switching features of the as-fabricated metal/Si_3N_4/n-GaN MIS device are not repeatable and retentional enough for the application as nonvolatile memory due to the conduction mechanism relating to the charge trapping and hopping or tunneling in Si_3N_4. Jiang et al. have demonstrated that the resistive switching effects could be improved in the annealed Si-rich SiN_x/SiN_y MIS device based on the mechanism of forming/rupturing continuous nanocrystalline silicon (nc-Si) pathways [31]. Shi et al. have revealed that the performances of Ta_2O_{5-x} resistive switching memory could be greatly improved by Gd-doping. The Gd-doping memory presented ultralow power operation, good data retention time, and high switching speeds for SET/RESET processes for the reason that the introduced Gd ions acted as oxygen trappers not only suppressing the generation of oxygen vacancy defects and increasing the Ta_2O_{5-x} resistance but also increasing the oxygen-ion migration barrier [32]. Guo et al. have investigated the resistive switching behaviors of Al-doped HfO_x films and observed much uniform distribution of resistance and good retention property due to the control of oxygen vacancies by Al dopants [33]. Liu et al. have improved the resistive switching properties of a ZrO_2-based memory by implanting Ti ions on account of the doped Ti impurities could improve the formation of conducting filaments and switching behaviors [34]. In short, it is expected to improve the performances of memristors by embedding specific dopants or nanoparticles. In order to improve the performances of our Ti/Si_3N_4/n-GaN memristor, the approach of *in-situ* local Ti doping in Si_3N_4 by thermal annealing is carried out and the effect of annealing on the bipolar resistive switching characteristics of the Ti/Si_3N_4/n-GaN MIS device is also investigated.

2. Experimental details

2.1. Preparation of n-GaN semiconductor

The n-type GaN semiconductor was grown on c-plane sapphire substrate by MOCVD. Trimethylgallium (TMGa) and ammonia (NH_3) were used as Ga and N precursors while silane (SiH_4) as the n-type dopant. Prior to growth, the c-plane sapphire substrate was thermally desorbed under H_2 for 10 min at 1100 °C. Then, a 36-nm-thick GaN buffer layer was deposited at 550 °C. Following the buffer layer, a 1-μm-thick undoped GaN layer and a 1-μm-thick Si-doped GaN layer were grown at 1050 °C. The carrier concentration and carrier mobility of the n-GaN layer were evaluated to be 8.6×10^{18} cm^{-3} and 236 cm^2 $(V\ s)^{-1}$ by Hall measurement equipment, under the conditions of applied current I = 5 μA and magnetic field intensity H = 7000 Gs.

2.2. Device fabrication

In the process of fabricating the Ti/Si_3N_4/n-GaN MIS device, a 100-nm-thick Si_3N_4 layer was firstly deposited on n-GaN using plasma enhanced chemical vapor deposition (PECVD) by reacting SiH_4 (40 sccm) and NH_3 (8 sccm) at 300 °C. Then, a series of Si_3N_4 mesas with diameter of 100 μm were left by reactive ion etching (RIE). On top of the Si_3N_4 mesas, Ti (100 nm) electrodes were fabricated using electron-beam evaporation and standard lift-off technique based on photolithography. The as-fabricated Ti/Si_3N_4/n-GaN MIS devices were annealed at 700 °C for 10 min in N_2 atmosphere.

2.3. Characterization and measurement

The electrical properties of the devices including the current-voltage curves (I-V), retention characteristic curves (I-t), and periodic Write-Read-Erase-Read (WRER) operation were measured by an Agilent B1500A semiconductor parameter analyzer with I/V power modules and waveform generator rapid measurement unit. The surface morphology of the device and its cross-section were characterized using a scanning electron microscope (SEM, Hitachi S-4800). The diffraction patterns of the devices were obtained by x-ray diffraction (XRD, Bruker D8). In addition, the SEM instrument was equipped with an energy dispersive x-ray spectrometer (EDS) for microanalysis. It was used to analyze the chemical elements of the Si_3N_4 layer. The depth profile analysis of the Ti/Si_3N_4/n-GaN sample annealed at 700 °C for 10 min is carried out by Auger electron spectroscopy (AES, Perkin-Elmer PHI 660). The current images of LRS and HRS were obtained by conductive force microscope (CFM, Shimadzu SPM-9700) operating in contact mode. Si cantilever (CONTPt-10, with Pt/Ir-coating and typical resonant frequency of 13 KHz) was used. Before the measurement of the current images for LRS and HRS by CFM, the Ti layer of Ti/Si_3N_4/n-GaN MIS device was removed by high energy neutral argon ion beam bombarding which is a physical etching method avoiding destroying the state of the Si_3N_4 layer. The chemical status of the Si_3N_4 layer is examined by x-ray photoelectron spectroscopy (XPS, ThermoVG, Sigma Probe).

3. Results and discussion

Fig. 1(a) shows the metallographic micrograph of the physical Ti/Si_3N_4/n-GaN MIS device arrays and the schematic configuration for a single cell (inset). The detailed fabrication process is depicted in the experimental section. In addition, its cross-sectional image obtained by scanning electron microscope (SEM) is also presented in Fig. 1(b), which intuitively confirms the device structure.

The typical I-V characteristic curves for the as-fabricated Ti/Si_3N_4/n-GaN MIS device are shown in Fig. 2(a). The compliance current (I_{cc}) is set to 10 mA to avoid a dielectric breakdown. In the process of measurement, the probe located at the n-GaN is defined as the common one, as shown in the inset of Fig. 2(a). The voltage applied to the Ti electrode is swept in a sequence indicated by red arrows numbered from 1 to 4. As can be seen in Fig. 2(a), the as-fabricated device switches from high resistance state (HRS) to low resistance state (LRS) when the applied voltage increases from

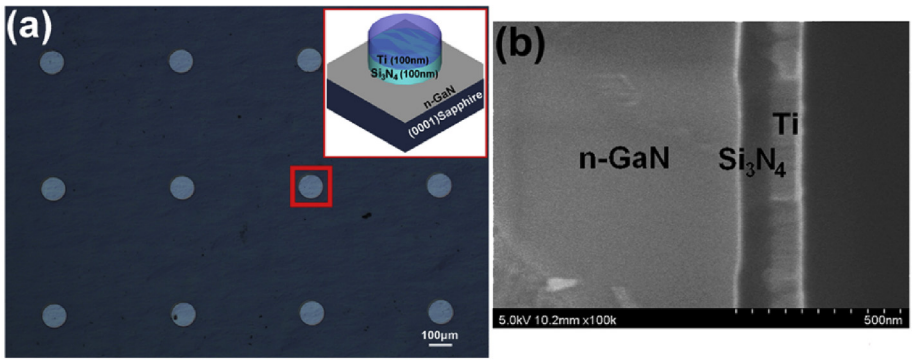

Fig. 1. (a) The metallographic micrograph of the physical Ti/Si_3N_4/n-GaN MIS devices. The inset shows the schematic configuration for a single cell. (b) Cross-sectional SEM image.

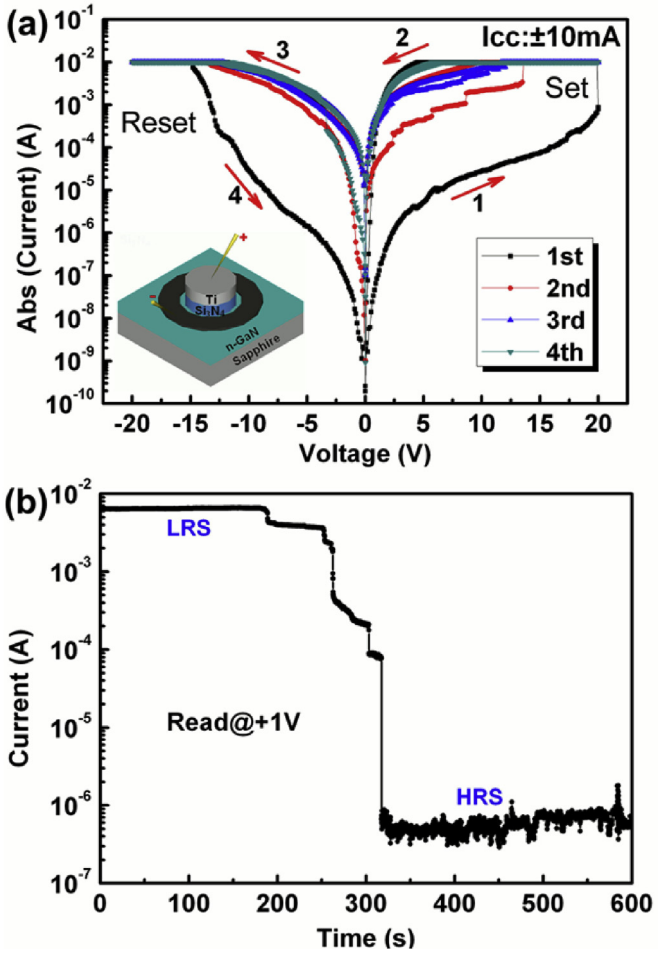

Fig. 2. (a) The repeatability test of I-V characteristic for the as-fabricated Ti/Si_3N_4/n-GaN MIS device. The sequence of sweeping voltage is pointed by red arrows numbered 1 to 4. The probe located at n-GaN was defined as common one, as shown in the inset. (b) The retention performance of the as-fabricated sample at the LRS which was read at +1 V. Before the retention performance measurement carrying out, the sample was undergoing the "SET" process. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

0 V to 20 V, which can be described as the "SET" process. The threshold voltage (V_{th}) of the "SET" process locates at about 20 V. The current decreases when the applied voltage sweeps backwards from −20 V to 0 V, which can be described as the "RESET" process (the transition from LRS to HRS), though the transition is not steep enough. It is worth mentioning that the high threshold voltage of the device mainly depends on the thickness of the Si_3N_4 layer. Viz., the as-fabricated Ti/Si_3N_4/n-GaN MIS device exhibits bipolar resistive switching characteristics at the initial measurement. However, unfortunately, the repeatability of the bipolar resistive switching characteristics for the as-fabricated Ti/Si_3N_4/n-GaN MIS device is very poor. We find that the resistive switching characteristics disappear with the repetitions and are almost ineffective after four repeated measurements.

Also, Fig. 2(b) shows the retention performance of the as-fabricated device at the LRS which are read at +1 V. Before the measurement carrying out, the device is applied a +20 V pulse to set into LRS and then read the current vs. time at +1 V. As can be seen, it keeps at LRS for only about 300 s and then turns into HRS spontaneously, which indicates the unreliable application as a nonvolatile memory.

In order to overcome the poor performances, the as-fabricated Ti/Si_3N_4/n-GaN MIS devices are thermally annealed at 700 °C for 10 min to realize *in-situ* local Ti doping. The x-ray diffraction (XRD) patterns before and after thermal treatment are presented in Fig. 3. In accordance with the Joint Committee for Powder Diffraction Standards (JCPDS), as shown in Fig. 3(a), the XRD pattern contains two peaks corresponding to (002) and (004) planes of hexagonal wurtzite-structure GaN (Card No. 50-0792), respectively. In Fig. 3(b), besides the characteristic peaks of n-GaN, the peaks labeled Green Triangle are well consistent with (102) and (103) planes of metal Ti (Card No. 65-3362) while the peaks labeled Red Circle are well consistent with (301), (320), (411), (420), (612), and (711) planes of the Si_3N_4 (Card No. 40-1129). Herein, we focus on the XRD pattern of the annealed Ti/Si_3N_4/n-GaN MIS device. As seen in Fig. 3(c), besides the characteristic peaks of n-GaN, Ti, Si_3N_4, two other kinds of characteristic peaks are observed. The peaks labeled Claret-red Prism are well consistent with (002), ($10\bar{1}$), and (102) planes of the TiN (Card No. 44-1095) while the peaks labeled Blue Square are consistent with (200), (221), and (113) planes of the Ti_5Si_3 (Card No. 29-1362). That is to say, through the thermal treatment, the top electrode (Ti) of the Ti/Si_3N_4/n-GaN MIS device will diffuse into Si_3N_4 dielectric layer through thermal diffusion and form TiN and Ti_5Si_3 phases, which is completely in agreement with the research results reported by Barbour et al. using Auger analysis [35]. To further demonstrate the *in-situ* local Ti doping by thermal treatment, the depth profile analysis is carried out by AES, as shown in Fig. 3 (d). As can been seen, at the interface of Ti/Si_3N_4, there forms a Ti-Si-N compound region, and the depth of Ti in Si_3N_4 layer is about 35 nm when Ti (100 nm)/Si_3N_4 (100 nm)/n-GaN sample is annealed at 700 °C for 10 min.

Fig. 4(a) presents the typical I-V characteristic curve of the annealed Ti/Si_3N_4/n-GaN MIS device in semi-logarithmic scale. The

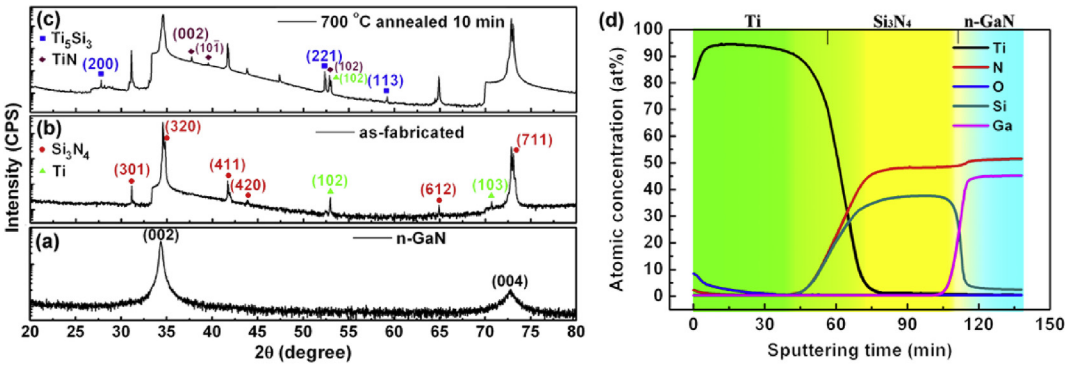

Fig. 3. The XRD patterns for (a) n-GaN, (b) as-fabricated Ti/Si_3N_4/n-GaN MIS device, and (c) Ti/Si_3N_4/n-GaN MIS device annealed at 700 °C for 10 min. (d) The corresponding depth profile analysis of the annealed device by Auger electron spectroscopy (AES).

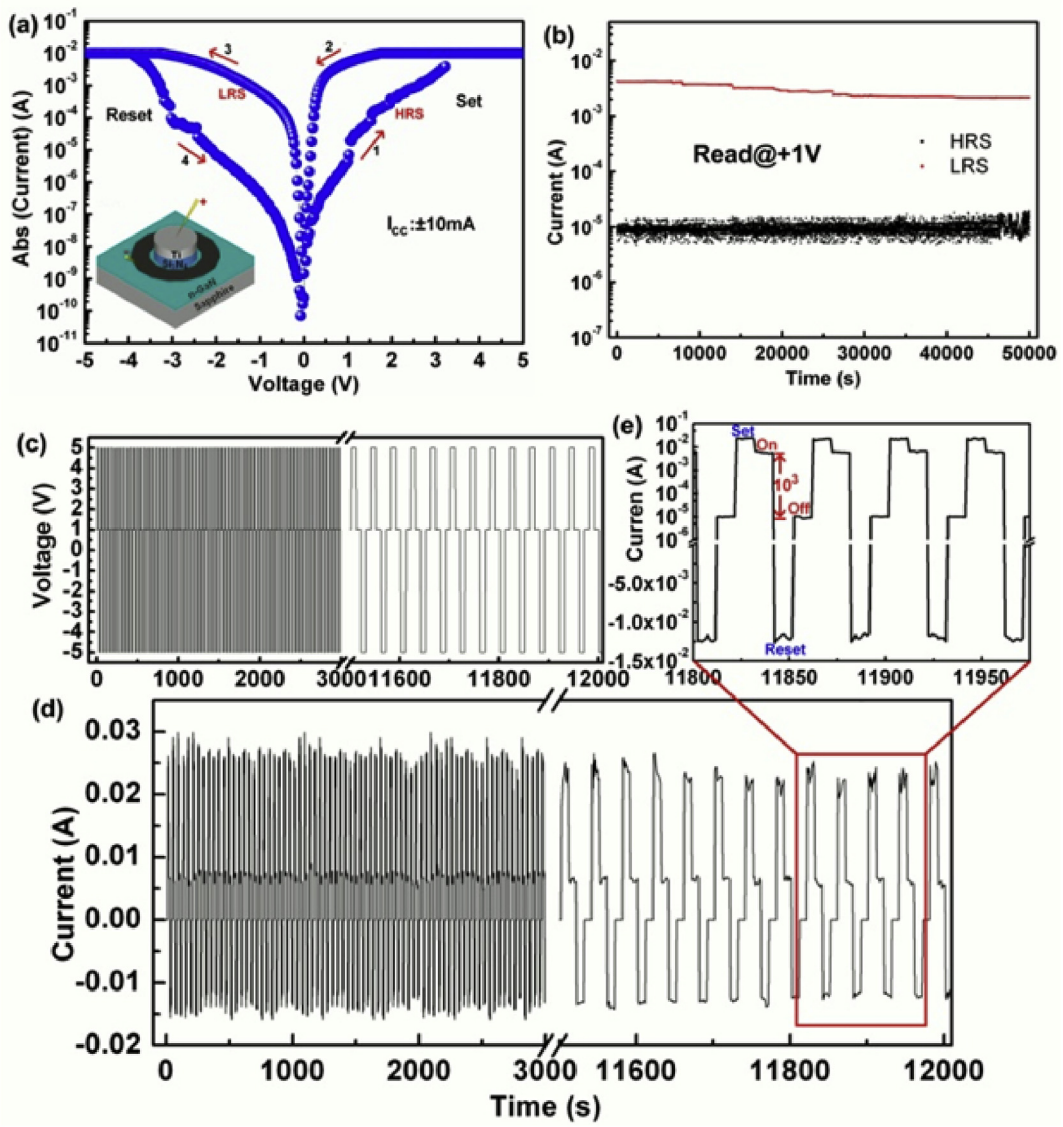

Fig. 4. (a) A typical I-V characteristic curve of the annealed Ti/Si_3N_4/n-GaN MIS device shown in semi-log scale. (b) The retention characteristics measured at V_{read} = 1 V for the LRS and HRS, respectively. (c) The Write-Read-Erase-Read (WRER) periods for the annealed Ti/Si_3N_4/n-GaN MIS device. The applied voltage cycles for writing (5.0 V), reading (1.0 V), erasing (−5.0 V), and reading (1.0 V). (d) The corresponding current cycles in linear scale for WRER process. (e) Partial enlarged view of current cycles in complex coordinate. The On/Off ratio was about 10^3.

I_{cc} is also set to 10 mA. During the measurement, the device switches from HRS to LRS when the applied voltage increases from 0 V to 5 V with a V_{th} about 3.2 V. Also, it switches from LRS to HRS when applying a negative voltage larger than −4 V. Viz., the annealed Ti/Si_3N_4/n-GaN MIS device still presents bipolar resistive switching characteristics. To elucidate the nonvolatile memory properties of the annealed device, the retention test is carried out by using a reading voltage (V_{read} = 1 V) after each one of a series of +5 V pulses to switch the device ON (writing process) and -5 V pulses to switch it OFF (erasing process). Thus, we observe an optimized retention time for HRS and LRS, as shown in Fig. 4(b). The endurance test of the device is also carried out under periodic Write-Read-Erase-Read (WRER) cycles (Fig. 4(c)). The corresponding current cycles in linear coordinate and partial enlarged view in complex coordinate for WRER process are shown in Fig. 4(d) and (e) respectively, which indicates the stability and repeatability of resistive switching behaviors. The ON/OFF ratio reaches up to 10^3. In addition, the threshold voltage of resistive switching is lower than that of the as-fabricated one, as seen in Fig. 2(a). Moreover, the resistive switching characteristics of the devices annealed under different conditions such as different temperature, different time are also demonstrated to further confirm the annealing effect (see Fig. S2 in Supplementary Materials). In short, compared with the devices of as-fabricated and annealed under different conditions, the bipolar resistive switching features are greatly optimized by annealing at 700 °C for 10 min.

For the purpose of understanding the mechanism of stable resistive switching in local Ti doping Si_3N_4 layer, conductive force microscopy (CFM) is adopted to probe the local conductive current of the film. Prior to the CFM scanning, the upper Ti metal presented in the cross-sectional SEM image (Fig. 5(a)) is removed by the method of ion beam etching, which is depicted in the experimental section in detail. In Fig. 5(b), the left and the right insets show the metallographic micrographs of a single cell annealed at 700 °C for 10 min before and after removing the upper Ti metal, respectively. To further confirm the Ti doping in Si_3N_4, the x-ray energy dispersive analysis (EDS) data is obtained from Si_3N_4 film of right inset, which agrees with the XRD and AES results. In our CFM setup, the n-GaN is always grounded through a metallic clamp and the voltage is applied to the scanning tip locating at the surface of Si_3N_4 film, as shown in Fig. 5(c). Before measurement of LRS, the annealed Ti/Si_3N_4/n-GaN MIS device is firstly switched from HRS to LRS by applying a +5 V pulse. Then, after removing the upper Ti metal by ion bombardment, we apply a reading voltage (V_{read}) of +1 V on the scanning tip and operate the scanning process in contact mode. The current image of Si_3N_4 layer under LRS is obtained in 5 × 5 μm^2 scanning area, as shown in Fig. 5(d). It shows that the Si_3N_4 layer under LRS presents a series of nanoscale conductive spots with a magnitude of current reaching up to tens of nA for a single one (partially highlighted by red circles). Thus, it confirms the presence of high density nano-filaments in the Si_3N_4 layer of LRS. On the contrary, when the annealed Ti/Si_3N_4/n-GaN MIS device undergoes a writing process by applying a +5 V pulse and an erasing process by applying a -5 V pulse in sequence, in other words, the device switches from HRS to LRS at first and then returns to HRS, we also obtain a current image of Si_3N_4 layer under HRS in 5 × 5 μm^2 scanning area by the method mentioned above. The result shown in Fig. 5(e) demonstrates that few nanoscale conductive spots are detected at V_{read} = 1 V which confirms the rupture of nano-filaments in Si_3N_4 layer. In short, the mechanism of stable resistive switching in local Ti doping Si_3N_4 layer can be ascribed to the formation and rupture of nanoscale filamentary-based conductive channels.

In fact, the Ti/Si_3N_4 composite film belongs to the Ti-Si-N material system after thermal treatment [36]. Based on the observed conductive behavior by nano-filaments, the stable resistive

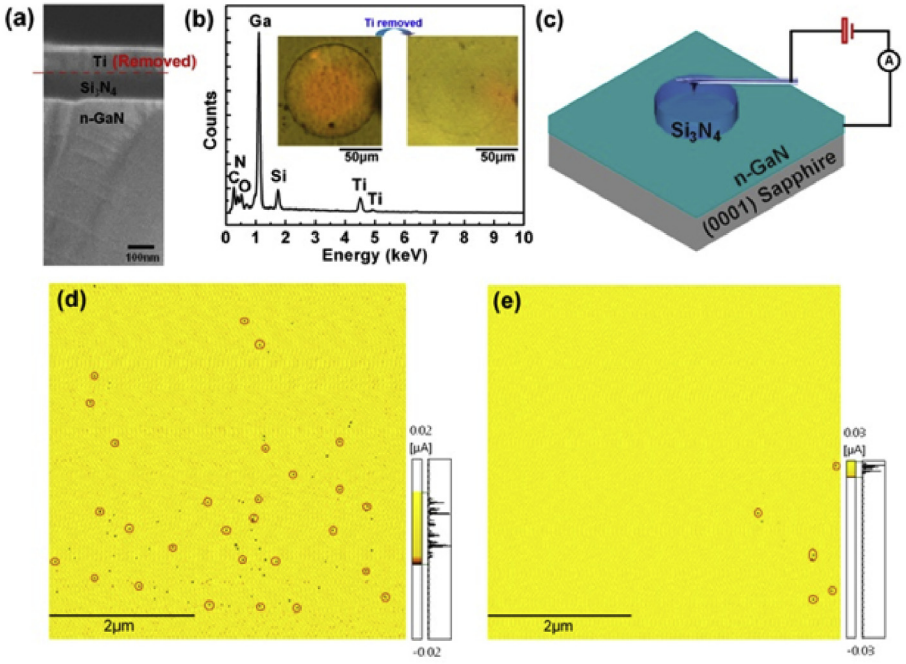

Fig. 5. Schematic of measuring the filamentary-based conductive channels by CFM. In the process, (a) the upper Ti metal presented in the cross-sectional SEM image is removed by the method of ion bombardment. (b) The insets showed the metallographic micrographs of a single cell annealed at 700 °C for 10 min before (left) and after (right) removing the upper Ti metal. The EDS data for the right inset. (c) CFM setup (It operates in contact mode. The scanning tip located at the surface of Si_3N_4 is biased while the counter-tip electrode contacts the border of the n-GaN). (d) The current image of LRS at V_{read} = 1 V after "Set" process. (e) The current image of HRS at V_{read} = 1 V after "Reset" process. The scanning area of Si_3N_4 is 5 × 5 μm^2.

switching can be proposed to be an electro-reductive process inducing the formation of silicon filaments which is similar to previous observation in the case of silicon oxide material system [10,37,38]. More precisely, the nanoscale silicon filaments are formed by Ti dopants assisted electro-reductive process. In order to confirm this viewpoint, XPS spectra for an annealed Ti/Si_3N_4/n-GaN MIS device under LRS with upper Ti metal removed is measured (see Fig. S3 in Supplementary Materials). The existence of the Ti^{2+}, T^{3+}, and Ti^{4+} states mainly result from the *in-situ* local Ti diffusion into Si_3N_4 by thermal treatment. Due to the lower binding energy of Ti-N bonds (about 2.2 eV) [39] than that of Si-N bonds (about 3.45 eV) [40], and the unstable Si-N bonds formed by intermediate states including Si^{1+}, Si^{2+}, Si^{3+} in annealed Ti/Si_3N_4 composite film which can be easily broken under high local electric field [41,42], the Ti dopants preferentially bond the N atoms to form Ti-N bonds under the writing process, decomposing Si^0 from Si_3N_4 in Si_3N_4 layer. The existence of Si^0 dominates the formation of the Si conductive nano-filaments observed by CAFM, as previously reported Si-filaments formation in the Si-rich SiN_x layer [30]. Once the Si conductive nano-filaments form, the device undergoes a transition from HRS to LRS. When applying a negative pulse (erasing process), the Si filaments on the side of n-GaN layer will firstly re-combine with nearby N atoms by redox process. It should be noted that due to the existence of Schottky barrier between the filaments and the n-GaN (as demonstrated in Fig. S4, Supplementary Materials), it needs a further same polar bias to make the Si filaments completely disconnect at the n-GaN side. Once finishing the disconnection, it will make the device turn into HRS. It is worth pointing out that the Si^0 decomposed from the Si-N bonds with the assistance of Ti dopants plays an important role in the formation of Si nano-filaments.

4. Conclusions

In summary, we have developed a nitride semiconductor compatible memristor based on Ti/Si_3N_4/n-GaN MIS structure. In order to improve the poor stable and repeatable bipolar resistive switching characteristics of the as-fabricated Ti/Si_3N_4/n-GaN MIS devices, a concept of *in-situ* local Ti doping in the Si_3N_4 insulator by annealing is proposed and carried out. By contrast, the annealed Ti/Si_3N_4/n-GaN MIS device performs better repeatability and stability than that of the as-fabricated one. The mechanism involved is also clarified by CFM and XPS, and can be ascribed to the local Ti dopants in the Si_3N_4 bonding the N atoms at positive bias by electro-reductive process which is facilitating to form stable nanoscale Si filaments, and the Si filaments will rupture by recombining with N atoms near the n-GaN side at negative bias. It is distinguished from the traditional charge trapping and hopping or tunneling in Si_3N_4. The proposed devices are easy to integrate with the GaN-based HEMTs to structure 1T1R nonvolatile memory cells, which will develop the application of the nitride semiconductors in the aspect of data storage.

Acknowledgments

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Appendix A. Supplementary data

Supplementary data related to this article can be found at https://doi.org/10.1016/j.jallcom.2018.01.072.

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