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Electronic Devices and Circuits Based on Wafer-Scale Polycrystalline Monolayer MoS_2 by Chemical Vapor Deposition

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2D layered materials such as graphene and transition-metal dichalcogenides (TMDCs) have emerged as promising candidates for next-generation nanoelectronic applications due to their atomically thin thicknesses and unique electronic properties. Among TMDCs, molybdenum disulfide (MoS_2) has been extensively investigated as a channel material for field-effect transistor (FET) and circuit realization. However, to date most reported works have been limited to exfoliated MoS_2 nanosheets primarily due to the difficulty in synthesizing large-area and high-quality MoS_2 thin film. A demonstration of wafer-scale monolayer MoS_2 synthesis is reported by chemical vapor deposition (CVD), enabling transistors, memristive memories, and integrated circuits to be realized simultaneously. Specifically, building on top-gated FETs with a high-κ gate dielectric (HfO_2), Boolean logic circuits including inverters and NAND gates are successfully demonstrated using direct-coupled FET logic technology, with typical inverters exhibiting a high voltage gain of 16, a large total noise margin of 0.72 V_{DD} at V_{DD} = 3 V, and perfect logic-level matching. Additionally, resistive switching is demonstrated in a MoS_2-based memristor, indicating that they have great potential for the development of resistive random-access memory. By virtue of scalable CVD growth capability, the way toward practical and large-scale electronic applications of MoS_2 is indicated.

1. Introduction

Recently, 2D layered materials (2DLMs) have emerged as promising candidates for next generation nanoelectronic applications owing to their unique electronic properties and ultrathin geometry.[1–3] The discovery of graphene has attracted intense attention due to its superior conductivity property. However, graphene is not a good choice for logic application because of its gapless nature, impeding the fabrication of devices with high on/off ratio or amplifiers requiring a voltage gain of >1.[4,5] To overcome the bandgap limitation, transition metal dichalcogenides, a different class of 2D materials, have been discovered and gained extensive research interest.[6,7] They usually consist of a layer of transition metal atoms (such as Mo, W, and Ti) sandwiched between two layers of chalcogen atoms (such as S, Se, and Te). Among them, molybdenum disulfide (MoS_2), due to its direct moderate bandgap (1.8 eV for monolayer) and high electron mobility, has become the most investigated 2DLM for realizing future-generation electronic and optoelectronic devices.[8] To date, functional devices such as field-effect transistors (FETs),[9–13] logic circuits,[14–18] and optoelectronic devices[19] based on MoS_2 have been widely demonstrated. For example, monolayer MoS_2-based transistors have been implemented with on/off ratios achieving 10^8 and electron mobility up to 320 $cm^2\ V^{-1}\ s^{-1}$.[9,15] However, most of the reported MoS_2 devices rely on mechanically exfoliated MoS_2 nanoflakes and a vast majority of them remain at the level of discrete transistors. Although exfoliated flakes are

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of high quality, the micromechanical cleavage approach lacks the systematic control of the 2D material in terms of thickness, size, and uniformity, thus hindering their actual integration into scalable device fabrication. To address such issue, considerable efforts have been dedicated to exploring large-scale growth of atomically thin MoS_2 films with controlled chemical composition and physical dimension. Until now, various approaches have been demonstrated including liquid exfoliation, atomic layer deposition (ALD), chemical vapor deposition (CVD), and metalorganic chemical vapor deposition (MOCVD).[20,21] For liquid exfoliation, although it could guarantee the production of a relatively large quantity of materials, it lacks a good control of the flake size and thickness, and the resulting materials tend to be contaminated with excessive impurity doping.[22] Regarding ALD process, it usually results in low crystallinity of the produced film.[23,24] Besides, highly uniform MoS_2 monolayer film was produced by a well-designed MOCVD process, but the use of vapor phase reactants makes the growth process more sophisticate.[25] In comparison, CVD process based on solid-phase precursors allows the growth of relatively high quality crystals with a well-controlled lateral size and layer thickness in a cost-effective way.[21,26] To date, significant progress has been made in growing large-area MoS_2 film of improved quality, by tuning of process parameters (operating pressure, temperature, concentrations of the chemical precursors, etc.), reactor geometry, and choice of chemical precursors, and by introducing seed promotors and gases such as oxygen.[27–30] However, few works have been done in regulating the flux and concentration gradient of the chemical precursors using reactive barriers. Meanwhile, despite the decent performance of individual MoS_2 transistor, higher level electronic circuits based on large-scale MoS_2 are required toward ultimate practical applications. Over the past years, the progress in CVD-growth of large-area atomically thin MoS_2 film renders it possible for the correlated realization of high-yield integrated circuits. Inspiringly, a microprocessor has recently been demonstrated on the basis of large-scale bilayer MoS_2 grown by CVD.[31] Nevertheless, the fabrication still required a complicated process of transferring the thin film onto a target substrate, similar to many reported MoS_2 works.[17,32,33]

Here, we report a scalable approach to fabricating fundamental building blocks of digital electronic circuits using large scale monolayer MoS_2 synthesized via CVD. Particularly, for growing MoS_2 film, an additional Ni foam is added as a barrier to limit the deposition rate of chemical precursors, which enables an even distribution of reactants on the substrate for achieving continuous MoS_2 film with improved quality. Then we fabricated transistors on the as-grown MoS_2 in a straightforward manner without a transfer process, thus ensuring the entire fabrication process fully compatible with existing Si technology. The resultant transistors exhibit promising performance with a high on/off ratio up to 10^6 and a subthreshold swing of ≈130 mV dec^{-1}, indicating a good control over short channel effect. Apart from discrete transistors, Boolean logic functions including NOT (or inverter) and NAND gates are demonstrated using direct-coupled FET logic (DCFL) technology through a careful circuit design. The inverter exhibits a voltage-match characteristic and a high voltage gain of ≈16 at V_{DD} = 3 V. Particularly, the noise margin of 0.41 V_{DD} for low input voltage (NM_L) and 0.31 V_{DD} for high input voltage (NM_H) manifest its suitability for realizing complex cascaded circuits. Additionally, we show the existence of resistive switching behavior in MoS_2 transistor-based structure, implying its high potential for resistive random access memory-relevant application such as neuromorphic computing.

2. Results and Discussion

2.1. Monolayer MoS_2 Thin Film Synthesis

The monolayer MoS_2 was synthesized on a commercially available c-plane (0001) sapphire substrate in a quartz tube furnace. Compared with SiO_2, the use of sapphire as substrate is expected to result in MoS_2 film growth of higher quality, owing to its single crystal structure and the commensurability of the sapphire lattice with MoS_2.[34,35] MoO_3 and sulfur were used as the precursors. **Figure 1**a,b schematically illustrates the arrangement of our tube furnace for the MoS_2 growth. Different from previous works of CVD-grown MoS_2, a Ni foam was employed to serve as the reactive barriers for limiting the deposition rate of the chemical precursors. Ni is known to react with MoO_3, thus it functions not only as a physical barrier but also as a chemically reactive trap of MoO_3, which allows greater regulation of the precursor flux during the growth process compared with an inert physical barrier, hence the growth of MoS_2 film with improved quality. Additionally, we noticed that the absence of a Ni foam would result in a reduced coverage of 2D MoS_2 on the substrate.

An optical image of the CVD-grown MoS_2 film on a 1/4 2-inch transparent sapphire substrate is shown in Figure 1c. Following the growth, Raman and photoluminescence (PL) measurements were performed on selected regions (Figure 1d) at room temperature with a 532 nm laser for excitation. As shown in Figure 1e, two Raman peaks are observed at 386.5 and 406.1 cm^{-1}, corresponding to the E_{2g} and A_{1g} vibration modes of MoS_2, respectively. Furthermore, the separation of 19.6 cm^{-1} between the E_{2g} and A_{1g} mode peaks confirms the monolayer nature of the grown film, whereas the larger separation of 23.2 cm^{-1} of the two modes indicates the formation of few-layer MoS_2 (the gray dots as shown in Figure 1d) during the growth process. The ratio of the monolayer area to the entire MoS_2 film was estimated to be 82.7%, evidencing the dominance of monolayer MoS_2 growth (Section S1, Supporting Information). One future direction to reduce few-layer MoS_2 growth is to identify the process window in which a complete MoS_2 monolayer emerges prior to the development of few-layer islands, through further tuning the synthesis parameters. In Figure 1f, the PL peak at the wavelength of ≈657 nm is observed, which is consistent with the ≈1.8 eV bandgap for monolayer MoS_2. Besides, the PL intensity for monolayer MoS_2 is more than one order higher than for the few-layer MoS_2, as a result of their respectively direct and indirect bandgaps. Furthermore, the relatively high uniformity of the single layer film has been revealed by PL mapping over a 20 μm × 20 μm region (Section S1, Supporting Information).

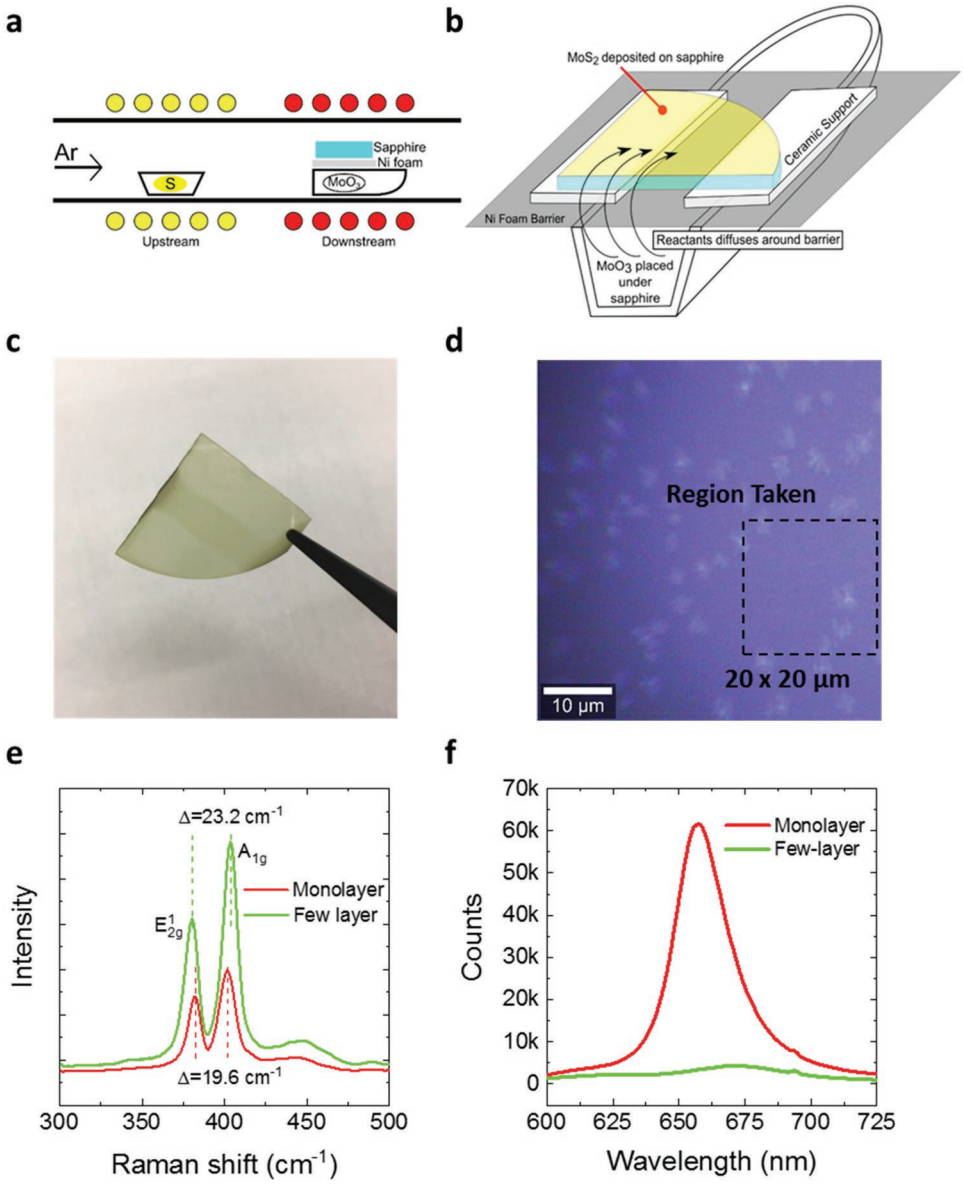

Figure 1. Growth and material characterization of the large-scale CVD-grown monolayer MoS_2 film. a) Crucible placements in tube furnace for MoS_2 growth with sulfur (S) and MoO_3 in the upstream and downstream regions, respectively. b) An illustration of detailed arrangement of the substrate, precursor flow, and Ni foam for MoO_3-containing crucible. c) Optical image of the monolayer MoS_2 thin film on a quarter 2-inch sapphire substrate. d) Optical image of the chosen region for the measurement. e) Raman spectrum of the monolayer and few-layer MoS_2 within the grown film. The 19.6 and 23.2 cm^{-1} distance between the A_{1g} and E^1_{2g} peaks correspond to monolayer MoS_2 and few-layer MoS_2, respectively. f) Photoluminescence (PL) spectrum of the MoS_2 film. The PL intensity for monolayer MoS_2 is much higher than for the few-layer MoS_2, as a result of their respective direct and indirect bandgaps.

2.2. Device Fabrication

Electronic devices and circuits were directly fabricated from the as-grown monolayer MoS_2. Active regions for transistors were defined in a patterning step followed by a CHF_3-based reactive ion etching process. After that, 5 nm/70 nm Ti/Au source/drain electrodes were formed by electron beam evaporation following another patterning step. Because of the insulating substrate, we employed top-gate architecture for the device fabrication, which is considered being more compatible with the existing technology. A 20 nm thick HfO_2 with a permittivity of 15 was grown by ALD at 150 °C to serve as gate dielectric (Section S2, Supporting Information). Finally, another 5 nm/70 nm Ti/Au was deposited followed by a standard lift-off process to form the top-gate electrode. Particularly, for logic circuits, a via-hole connecting the source and gate terminals of the pull-up transistor was defined prior to the gate metal deposition. A schematic of the MoS_2-based top-gated transistors is given in **Figure 2**a and more details on the fabrication process can be found in the Experimental Section.

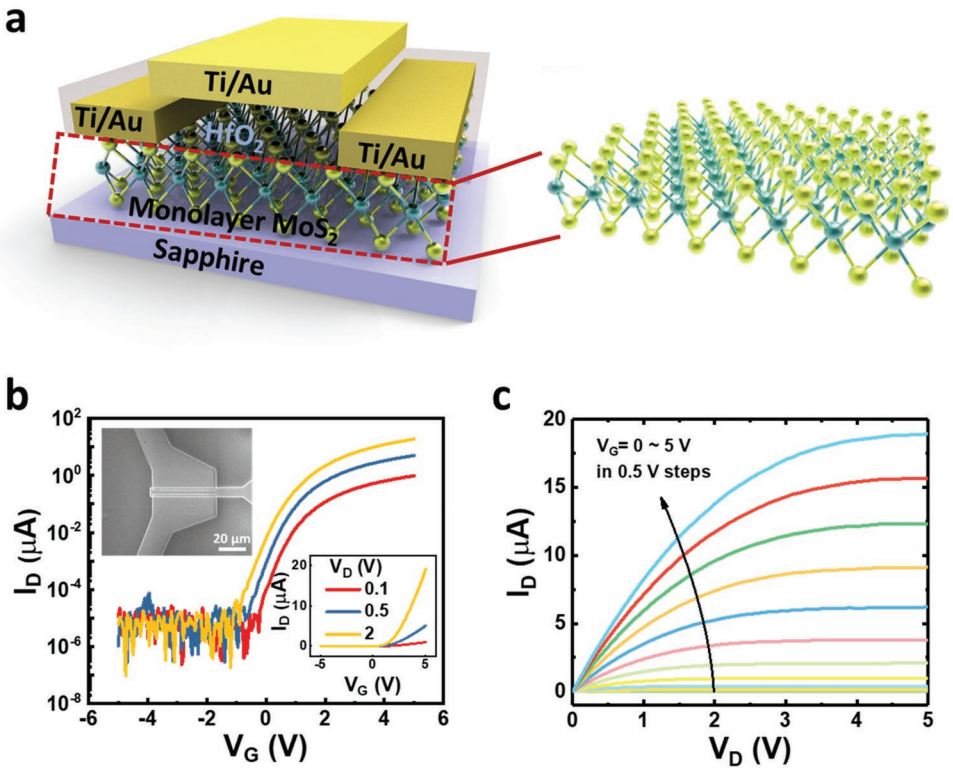

Figure 2. Characterization of a representative MoS_2 transistor. a) Schematic of the top-gated MoS_2 transistor. b) Transfer characteristics of the device, showing an evident n-type behavior with a high on/off ratio up to 10^6 and a low subthreshold swing (SS) of 130 mV dec^{-1}. Inset is a scanning electron microscope (SEM) image of the device. c) Output characteristics (I_D–V_D) of the device. The current saturates at $V_D = 5$ V.

2.3. Characterization of MoS_2 Field-Effect Transistors

We first investigated the electrical properties of the MoS_2 transistors. A 6 × 6 array of MoS_2 transistors were fabricated over a 2 mm × 3 mm area (Section S3, Supporting Information), with a channel length (L) of 3 μm and a channel width (W) of 45 μm. The transfer characteristics of a representative MoS_2 transistor at different drain biases are plotted in Figure 2b. Apparently, the MoS_2 FET exhibits a typical n-type conduction behavior with a current on/off ratio exceeding 10^6 that is sufficient for logic circuits application.[14] By using the equation $SS = (d \log_{10} I_D/dV_G)^{-1}$, where V_G is the gate bias and I_D is the drain–source current, a small subthreshold swing of ≈130 mV dec^{-1} is determined. This value indicates a steep switching characteristic of the device and is likely to be further reduced by downscaling the dielectric thickness. Furthermore, the field-effect electron mobility is extracted by using the equation $\mu_{FE} = g_m \times (L/WC_{OX}V_D)$, where g_m is the transconductance of the transistor, C_{OX} is the capacitance of gate dielectric per unit area, and V_D is the drain to source voltage bias. For the fabricated transistors, typical electron mobility is in the range from 0.1 to 1 $cm^2\ V^{-1}\ s^{-1}$, with the highest value reaching 3 $cm^2\ V^{-1}\ s^{-1}$ (Section S4, Supporting Information). These values are slightly lower than those in representative works on CVD-MoS_2[26,36] and can be ascribed to smaller monocrystalline domain sizes as well as sparse growth of few-layer MoS_2 islands that cause more significant carrier scattering. The low carrier mobility for CVD grown MoS_2 in comparison with exfoliated MoS_2 nanoflakes can be attributed to intrinsic defects, grain boundaries, as well as interface scattering due to the atomically thin nature of the film, which highlights the demand of further advancement in the material synthesis toward practical application. One way to enhance the charge mobility is to increase monocrystalline domain sizes for reduction of grain boundary scattering. This can be potentially realized by having a separate control of MoO_3 precursor powders and substrate temperature using a three-zone growth reactor. Consequently, individual heating temperatures can be applied to the substrate and MoO_3 source, where a lower temperature for MoO_3 is used to reduce MoO_3 sublimation and therefore MoS_2 nucleation density while adatom surface mobility is still high on the growth substrate at a higher temperature.[37] However, this strategy is beyond the capability of our setup at present stage. Alternatively, a transfer of the grown film to another substrate has proved helpful in improving device performance,[38] except that this would require a reliable and high throughput large scale transfer from grown substrate to target substrate.[39]

The output characteristics of the transistor at various top gate voltages from 0 to 5 V in a 0.5 V step are given in Figure 2c. The I_D–V_D curves show linear behavior at low drain bias voltages, indicating that a near-Ohmic contact is achieved as a result of the low potential barrier between Ti and MoS_2. More importantly, clear current saturation behavior is observed at high source–drain bias as featured by the close-to-zero drain–source conductance (as defined by $G_{DS} = dV_{DS}/dI_{DS}$), which is desired for logic circuit operation in this regime. In addition,

the well-matched onset of saturation and the gate overdrive suggest its potential for constructing circuits with logic-level matching characteristic.

2.4. Characterization of MoS_2 Based Boolean Logic Circuits

By leveraging on the discrete transistors, we then constructed integrated logic circuits based on the CVD-grown monolayer MoS_2. To this end, we have fabricated Boolean logic gates such as NOT and NAND gates, which form the fundamental building blocks for the realization of advanced digital circuits. The circuit was implemented by *N*-type metal-oxide-semiconductor logic in a similar way to the work in ref. [31], where both pull-up (load) and pull-down transistors were n-type enhancement-mode FETs. The gate and source electrodes of the pull-up transistor are connected together to serve as the output terminal. Such strategy allows us to design the width/length (W/L) ratios of the two FETs to achieve suitable switching threshold voltage as well as noise margin of the inverter, which are crucial to ensure the ability of constructing cascaded circuits. For example, two transistors with the same W/L ratio would cause a left shift of V_m and degrade the noise immunity. In our case, the W/L ratios were designed to be 50 μm/1.5 μm and 7 μm/3.5 μm for the pull-up transistor and the pull-down transistor, respectively, to shift V_m toward a more positive value for logic-level matching. The transfer characteristics of the two E-mode transistors are shown in **Figure 3**c. The more than ten times higher current for the pull-up FET in comparison to the pull-down FET manifests the successful control of device characteristics by geometrical scaling. The characteristics of the inverter are in principle determined by the output curves of the pull-down FET and the load curve of the pull-up FET (Figure 3d). Typically, the pull-down transistor operates in the triode regime or saturation regime, whereas the pull-up transistor operates in the subthreshold regime and acts as a current source over a large drain voltage range. The performance of a logic inverter is usually examined by its voltage transfer characteristics. As plotted in Figure 3e, the output signal of the inverter shows a clear opposite logic-level to its input voltage for a wide range of supply voltage V_{DD} from 2 to 4 V. The DC voltage gains, as defined by $V_{gain} = -dV_{OUT}/dV_{IN}$ which indicates the sensitivity of V_{out} switching to V_{in}, are extracted and plotted in Figure 3f. The highest gains are found to be 10, 16, and 19 for V_{DD} = 2, 3, and 4 V, respectively, which, being much larger than 1, indicates the ability of our n-logic inverter to serve as the building block of multistage circuits. Additionally, the noise margin plays a crucial role in determining the tolerance of an inverter to input signal noise and consequently the reliability of cascaded logic circuits. For our DCFL inverter, the noise margin for low input voltage and high input voltage are extracted to be $NM_L = 0.41\ V_{DD}$ and $NM_H = 0.31\ V_{DD}$ for V_{DD} = 3 V, respectively (Figure 3g). The noise margin of >30% for both NM_L and NM_H implies the potential of the inverter to be integrated into a complex circuit system. Besides, we performed the AC measurement on the inverter. Figure 3h shows the temporal evolution of V_{in} and V_{out} for a V_{DD} = 3 V at a frequency of 10 Hz. It is clear that the output curve is opposite to the input curve. For a more quantitative analysis on the switching performance of the inverter, the intrinsic delay time is determined by $\tau = RC_p$, where R is the transistor resistance corresponding to the transistor drive current and C_p is the overall parasitic capacitance. The parasitic capacitance C_p is mainly contributed by the gate capacitance of the two FETs, and can be calculated by $C_p = (L_1W_1 + L_2W_2)\varepsilon_r\varepsilon_0/t_{ox}$, where ε_r is the dielectric constant of HfO_2, t_{ox} is gate dielectric thickness, and ε_0 is the permittivity of free space. As a result, C_p = 0.66 pF is obtained. In addition, the peak drive current of the inverter at V_{dd} = 3 V is measured to be ≈35 nA. Therefore, the intrinsic delay can be estimated to be $\tau_{intrinsic} = C_pV_{DD}/I$ = 57 μs, indicating that the inverter can potentially operate at a maximum frequency of $f = 1/2\pi\tau$ = 2.8 kHz. Here it is to note that other factors such as imperfect Ohmic character at source/drain contacts and overlapping gate area larger than $L \times W$ of the device channels are likely to further degrade the switching frequency due to additional capacitive effect. We emphasize that similar to other works of integrated circuits based on large-scale MoS_2, the relatively low operation speed in this work is primarily a consequence of the low carrier mobility and the large parasitic capacitance resulted from large gating area. Consequently, improvement in frequency performance can be anticipated by shortening the device channel length to reduce simultaneously the gate capacitance and the channel resistance. Substantially, improving the film quality to enable a higher carrier mobility is necessary for the enhancement of the performance of MoS_2 circuits toward their realistic application in digital electronics. Furthermore, we compared our device with other reported MoS_2-based inverters (Section S5, Supporting Information). It is noticed that our logic circuit can deliver a decent voltage gain and matched logic voltage. Furthermore, while most of the reported MoS_2 based inverters relied on exfoliated MoS_2 flakes or required a complicated transfer process, thus being incompatible with existing Si technology, our work demonstrates a more practical and scalable approach to realizing large scale MoS_2 integrated circuits through a straightforward fabrication process on the as-used substrate.

Next, we further demonstrate a two-input Boolean NAND gate, which represents one of the two basic logic gates (together with NOR gate) with universal functionality. **Figure 4**a shows the schematic of the fabricated NAND circuit. The two-input NAND gate was implemented by connecting two pull-down transistors in series with the identical dimension of W/L (2 × 7.5 μm/3.5 μm) to maintain logic-level matching. The Boolean expression and NAND gate function are described in Figure 4b and the optical image of the NAND is given in Figure 4c. Figure 4d shows the timing diagram of the NAND gate. Apparently, it outputs a low logic state only when both input voltages are at high logic level. In contrast, with either or both inputs being equal to 0 V (logic state 0), the output voltage is approaching 3 V supply voltage V_{DD} (i.e., logic state 1) because at least one of the two pull-down transistors is forbidding current flow. Thus, the result demonstrates clearly the functionality of an NAND gate. Since more complicated logic circuits including other types of logic gates can be implemented using a combination of NAND gates, it is therefore plausible to manufacture fully integrated logic circuits based on large-scale CVD-grown monolayer MoS_2.

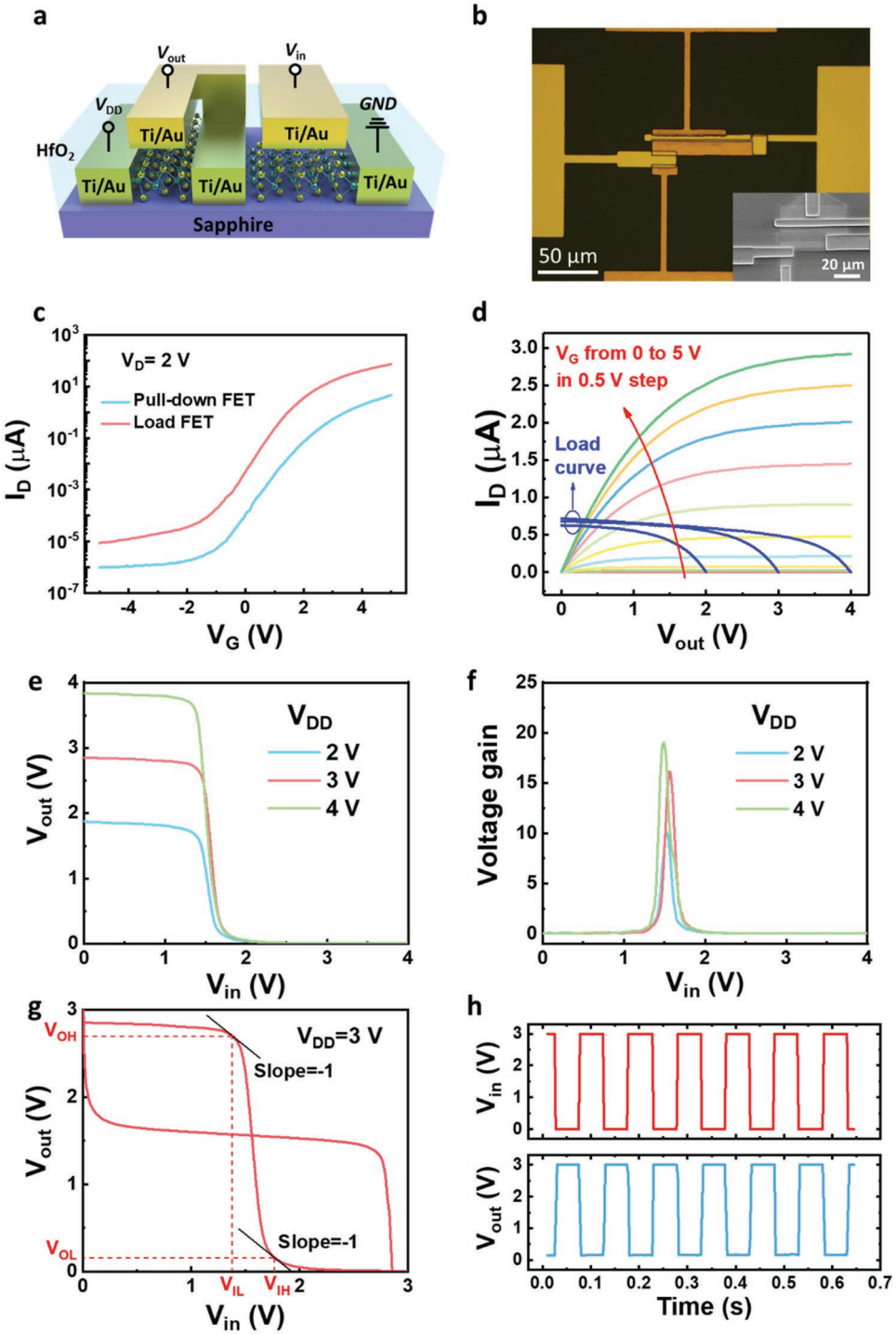

Figure 3. Characterization of the MoS_2-based logic inverter. a) Schematic and b) an optical image of the n-logic MoS_2-based inverter. Inset in (b) is an SEM image of the circuit. c) Transfer characteristics of the two FETs for inverter design. d) Output characteristics of the pull-down FET plotted together with load curves of the inverter for V_{DD} = 2, 3, and 4 V, respectively. e) Transfer characteristics of the inverter. The voltage is well matched with a supply bias ranging from 2 to 4 V. f) Voltage gain as a function of input voltage of the inverter. A high gain of 19 is achieved at V_{DD} = 4 V. g) Noise margin properties of the inverter. The extracted noise margins are 0.41 V_{DD} and 0.31 V_{DD} for NM_L (= $V_{IL} - V_{OL}$) and NM_H (= $V_{OH} - V_{IH}$), respectively, indicating a good tolerance to noise. h) Dynamic response of the inverter at a frequency of 10 Hz, showing unambiguously the inversion functionality.

2.5. Characterization of MoS_2 Based Memristive Memory

Over the past decade, memristors have been demonstrated and considered as an important candidate for future electronics for novel computing technologies such as in-memory computing and neuromorphic computing.[40,41] In recent years, 2DLMs have started to attract intense research interest for their potential in memristive device application. For instance, they can

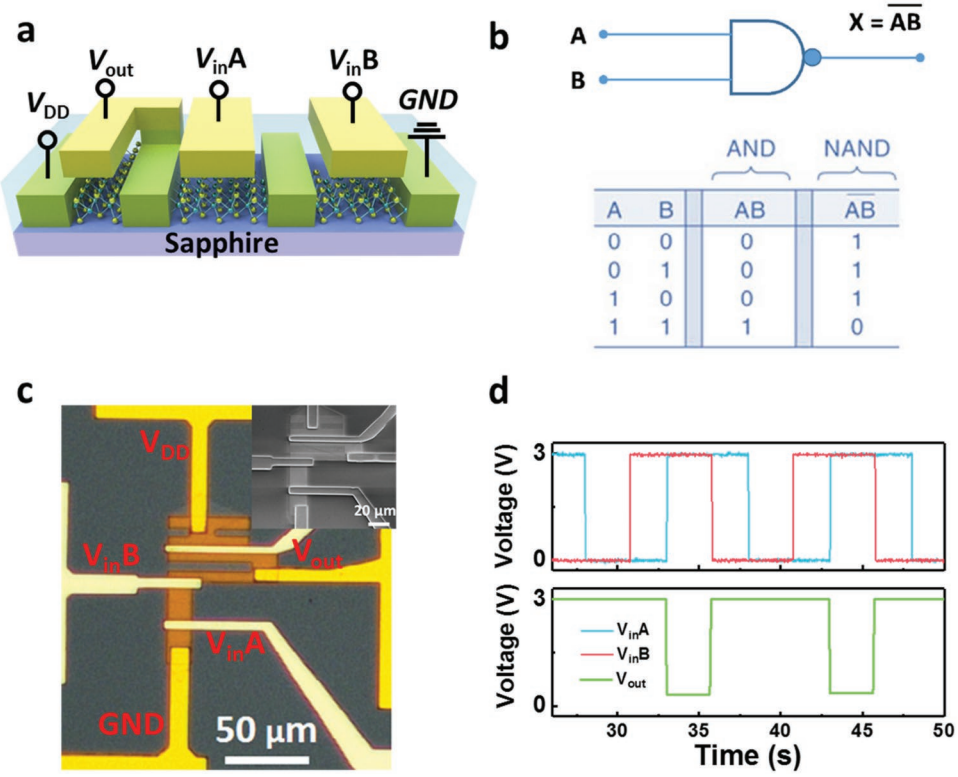

Figure 4. Characterization of the MoS_2-based NAND gate realized in this work. a) Schematic of the NAND gate. b) Boolean expression and logic function of the NAND gate. The NAND gate outputs a logic low voltage only when both the input voltages are at a logic high voltage. c) Optical image of the NAND gate. Inset is an SEM image of the circuit. d) Timing diagram of the NAND gate. The device outputs a high level of 3 V when either or both of the inputs are at 0 V.

be used as the core switching medium in metal–insulator–metal-structured two-terminal devices.[42–44] Particularly, among various 2D materials, polycrystalline MoS_2 synthesized by CVD has shown the prospect in fabricating memristive components.[45–47] Next, we show that the MoS_2 transistors can be exploited as memristive device with resistive switching characteristics. For this purpose, we investigated the electrical characteristics of a representative MoS_2 transistor. In **Figure 5**a, when the V_D is swept from 0 to 10 V, the device is gradually switched from the high resistance state (HRS) to the low resistance state (LRS). The LRS is maintained for V_D sweep from 10 V back to 0 V. Then a reset to the HRS is achieved through a V_D sweep from 0 to −10 V, and the device retains its HRS during the sweep from −10 to 0 V. Such a state evolution in a closed-loop of V_D sweep clearly manifests a bipolar analogue resistive switching behavior. The endurance characteristics of the device are examined by switching it between HRS and LRS in a consecutive 500 sweep cycles (Figure 5b). Based on this result, the resistance values corresponding to the HRS and LRS of the device are extracted at V_D = 0.1 V and plotted as a function of sweep cycles, as shown in Figure 5c. The switching ratio, defined as R_{HRS}/R_{LRS}, is calculated to be higher than 10, which is well comparable to previous work while using a much smaller voltage range.[45] We notice that by integrating an additional terminal, the memristors in our work is different from two-terminal memristive devices such as traditional TiO_2-based ones and recently demonstrated MoS_2-based atomristors.[42,48] Although the switching ratio might not be as high as in two-terminal memristors exhibiting abrupt resistance switching, the different structure is likely to provide new functionality that is inaccessible by two-terminal devices and will be exploited in our future work.[45] The resistive switching behavior can be attributed to the dynamic migration of the defects within the channel material. Indeed, various defects in MoS_2 have been observed experimentally in CVD-synthesized MoS_2 film, such as, single vacancy S (V_S), double vacancy S (V_{2S}), (5|7) Mo-Mo dislocation and (4|6) defect complex comprising a (5|7) S–S dislocation, and a double S vacancy V_{2S}.[49–51] In this work, the grown film was characterized by atomic force microscopy, and grain boundaries with 1–3 µm domain sizes have been revealed (Section S6, Supporting Information). Upon applying an external electric field, they will migrate favorably along grain boundaries toward or far from the electrode end of the device (depending on the bias polarity), resulting in dynamic tuning of the Schottky barrier heights and consequently resistance switching, as has been experimentally evidenced in polycrystalline MoS_2 devices on a Si/SiO_2 substrate.[45] In this regard, the switching behavior might vary from cycle to cycle due to the motions of defects taking place on the microscopic scale, which is common in different types of memristive devices.[43,52] Nevertheless, our device exhibits distinct resistance states over the 500 switching cycles, demonstrating its good endurance property. Further optimization of the performance will require a more-controllable defects engineering during as well as after the growth of the film.

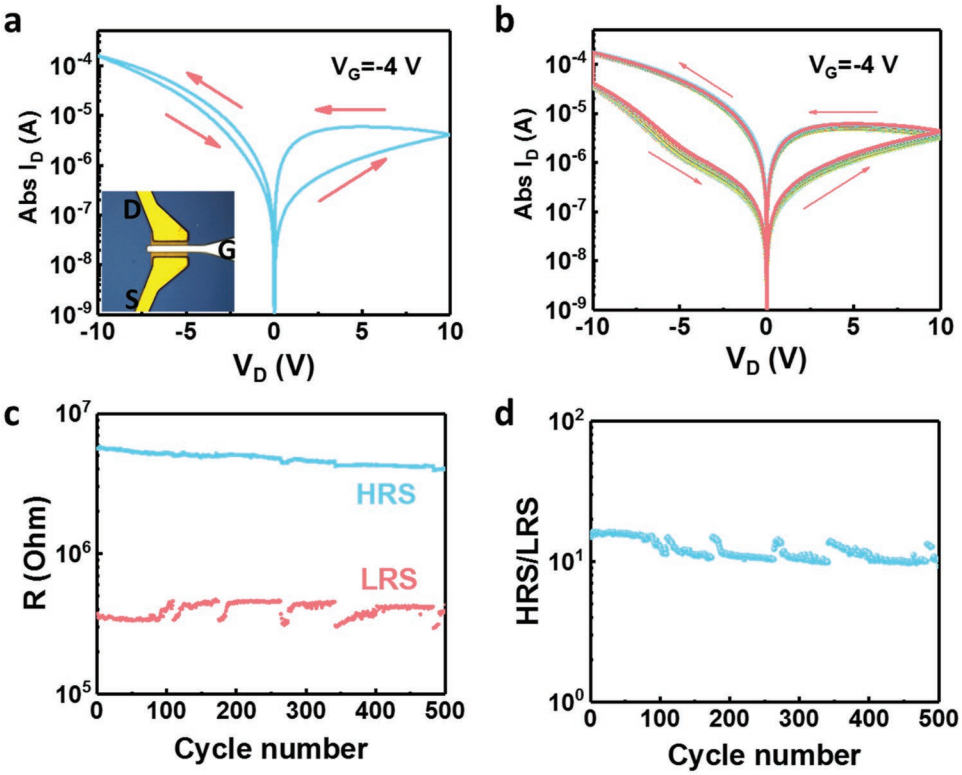

Figure 5. Resistive switching behavior observed in top-gated transistor made from CVD-grown monolayer MoS_2. a) Drain current (I_D) of a MoS_2 transistor ($W = 25$ µm, $L = 1.5$ µm) as a function of the drain bias (V_D) at a gate voltage of −4 V. The direction of V_D sweep is indicated by red arrows. Inset shows an optical image of the device. b) I_D–V_D curves for 500 consecutive sweeps at $V_G = -4$ V for the same device. The direction of V_D sweep is indicated by red arrows. c) Extracted resistance values corresponding to the high resistance state (HRS) and low resistance state (LRS) of the device as a function of sweep cycle number. The currents at $V_D = 0.1$ V in (b) are used for calculation. d) Switching ratio (defined by R_{HRS}/R_{LRS}) as a function of the sweep cycle.

3. Conclusion

In conclusion, we have demonstrated a practical approach to realizing fundamental building blocks for digital electronics based on large-scale monolayer MoS_2 film synthesized via a CVD process. Top-gated MoS_2 transistors with a thin high-κ gate dielectric were demonstrated, which exhibit an on/off ratio exceeding 10^6 and a subthreshold swing of ≈130 mV dec^{-1}, indicating a superior control of short channel effect over the widely explored back-gated transistor structure with thick SiO_2 gate oxide. By leveraging on DCFL technology, Boolean logic circuits including NOT (or inverters) and NAND gates were successfully realized, with the inverter achieving a high voltage gain of 16 and a large noise margin of 0.72 V_{DD}. Additionally, the potential of MoS_2-based transistors for memristive switching functionality was demonstrated, which holds promise for the development of neuromorphic computing architectures. This work paves the way toward realizing a fully integrated 2D electronics circuits with complex functionality and scalability based on CVD-grown monolayer MoS_2.

4. Experimental Section

Chemical Vapor Deposition of MoS_2: MoS_2 is deposited on a commercially bought c-plane (0001) sapphire (Al_2O_3) substrate (Namiki Inc) in a quartz tube furnace (planarTECH LLC) with two separate upstream and downstream heating zones. In the downstream region, 4.5 mg of MoO_3 (99.98%, Sigma-Aldrich) is placed in a single open-end crucible with a piece of nickel foam (size 3.5 cm × 3 cm, 1 mm thickness with 400 µm average pore size) placed directly above the MoO_3 powder. The sapphire is placed above the nickel foam, supported by two ceramic pieces. The arrangement of the MoO_3 crucible, nickel foam, and sapphire is similar to our previous work.[53] 950 mg of sulfur (99.998%, Sigma-Aldrich) is placed in the upstream zone, 40 cm away from the MoO_3 precursor.

The detailed process flow is as follow: The downstream region is first heated to 250 °C for 10 min for degassing purpose with the upstream zone kept at room temperature while an Ar flow of 200 sccm is maintained. The temperature is then ramped to 750 °C over 12 min and is maintained for an additional 13 min with an Ar flow of 50 sccm to allow MoS_2 deposition to occur. Afterward, the tube is allowed to naturally cool down to 650 °C prior to opening of the furnace heaters for rapid cooling through ambient exposure while the Ar flow is increased to 200 sccm. The pressure is maintained at 6 Torr during the entire process. This low pressure enviroment is considered the primary factor responsible for the growth of small domain sizes, in comparison with MoS_2 synthesis at a higher pressure.[53] It is to note that the relatively fast growth of MoS_2 film, in comparison with other works which might take much longer time,[39] is readily a result of the use of powder source as well as a much higher flux.

Device Fabrication: The device fabrication on sapphire substrate consisted of the following steps: First, metal markers for alignment purpose throughout the device fabrication process were fabricated by electron beam lithography (EBL: JOEL-6300FS) and subsequent metal deposition and lift-off process. Second, to define the active regions

for transistor fabrication, another patterning process was performed by Laser Writer (LW405B), and MoS_2 film was selectively etched by CHF_3-based reactive-ion etching (RIE) technique. Third, 5/70 nm Ti/Au source/drain electrodes were formed using Laser Writer patterning followed by metal deposition (E-beam evaporation) and lift-off process. In the fourth step, 20 nm thick HfO_2 was grown by ALD in a Cambridge NanoTech reactor at 150 °C to serve as the high-κ top-gate dielectric, where tetrakis(dimethylamido)hafnium [$Hf(NMe_2)_4$] and H_2O were used as the precursors and nitrogen (N_2) as the carrier gas.[54] The sequence of pulses for one deposition cycle of HfO_2 is H_2O (0.015 s)/N_2 (20 s)/$Hf(NMe_2)_4$ (0.15 s)/N_2 (30 s). Prior to top gate metal formation, Ar_2-based plasma was used to define the via-holes that connect the source/drain metal and top-gate metal layers where necessary. Finally, after electrodes patterning by Laser Writer, 5/70 nm Ti/Au top metal layer was formed by E-beam evaporation and subsequent lift-off process in acetone. During the fabrication, poly(methyl methacrylate) was used as photoresist for EBL and AZ1512 photoresist was used for Laser Writer patterning.

Electrical Characterization: All electrical measurements were carried out in air at room temperature. The current–voltage characteristics of the transistor and voltage transfer characteristics of logic gates were measured using a Cascade probe station with a HP4155B semiconductor parameter analyzer. For dynamic characterization, a digital waveform generator was used as the input source and the output signal was detected by a digital oscilloscope.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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