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Vertical GaN-on-GaN PIN diodes fabricated on free-standing GaN wafer using an ammonothermal method

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ABSTRACT

We report vertical GaN-on-GaN PIN diodes with a record high figure-of-merit (V_{BR}^2/R_{on}) of 29.7 GW/cm^2 on free-standing GaN wafer using a complementary metal-oxide-semiconductor (CMOS) compatible contact materials. Due to the low substrate resistivity, low contact resistance, and high quality of GaN drift layer, a low on-state resistance R_{on} of 0.31 mΩ cm^2 is obtained. With integrating of the metal filed plate structure in the vertical device, the peak electrical field along the GaN mesa edge can be significantly reduced, thus leading to a high breakdown voltage V_{BR} of 3.04 kV. The vertical GaN-on-GaN PIN diodes in this work show turn-on voltage V_{on} of ~3.4 V, on/off current ratio of ~1.3 × 10^7, and ideal factor n of ~2.2. According to the reverse switching measurement, the reverse recovery time T_{rr} (reverse recovery charge Q_{rr}) is 22.8 ns (4.8 nC) and 24.0 ns (5.4 nC), respectively, under a testing temperature of 300 K and 500 K.

1. Introduction

Gallium nitride (GaN) has shown to be promising for high voltage, high power, and high frequency applications, mainly due to its large bandap (~3.4 eV), high breakdown electric field (~3.3 MV/cm), and high saturation-drift velocity (~3 × 10^7 cm/s) [1–5]. As compared with the lateral GaN-based devices, vertical GaN-based devices are capable of handling larger current with a given device foot-print, or more efficient chip area utilization, and less susceptibility to the surface trap [6–13]. Due to the rapid development of high quality free standing GaN material growth by hydride vapor phase epitaxy (HVPE) [14,15], and ammonothermal method [16], the surface threading dislocation has been significantly reduced down to ~10^4-10^5 cm^{-2}, which further leads to a remarkable improvement in vertical GaN PIN diodes and Schottky barrier diodes (SBDs) [17]. Using multiple Si doped GaN drift to reduce the peak electrical field of PIN interface, the vertical GaN-on-GaN PIN diodes with V_{BR} of 4700 V has been demonstrated [10]. Due to the high level injection and photon recycling effect, the vertical GaN-on-GaN PIN diodes with low R_{on} of ~1.25 mΩ.cm [2] and the figure-of-merit (V_{BR}^2/R_{on}) of ~10 GW/cm^2 have also been obtained [13].

The breakdown voltage of vertical GaN-on-GaN PIN diodes can be enhanced through local electrical field modulating using various termination techniques, among which the metal field plate structure is the most effective to reduce the peak electrical field [12]. One step or two step mesa structure formed by reactive ion etching (RIE) is often used to isolate the devices with each other [2].

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However, RIE formation process can result in the surface damage (ions residues, nitrogen vacancies, etc), which can lead to a premature device breakdown. Dielectric layer form by plasma-enhanced chemical vapor deposition (PECVD), such as SiO_x or SiN_x film, can help to passivate the exposed GaN surface [7]. Also, low damage dielectric layer formation process, such as spin-on-glass (SOG), is also proposed to passivate the GaN surface and increase the device breakdown voltage [13]. N implantation into SiN_x passivation film is also proven to be effective termination method to locally modulate the peak electric filed [11]. For power device, thermal resistance of vertical devices is also extremely important of device under high power or high temperature operation. In order to eliminate the thermal resistance associated to the bulk GaN substrate, eiptaxial lift-off (ELO) technique has been proposed to transfer the active PIN diodes to a metal substrate (Cu) [18].

Cost-effective manufacture is a must for GaN-based device to be accepted in the commercial market. If the fabrication process of GaN-based device is compatible with the mainstream of silicon manufacture line, this can leverage the advantage of advanced silicon process technologies, further make GaN-based devices very competitive in the power device market. In the literature, gold is used as the anode or cathode metal for the GaN-based device. However, gold, as deep level impurity for silicon material, is prohibited in the silicon foundry. To develop GaN fabrication process using silicon CMOS compatible material is critical for GaN-based device commercialization in the future. In this work, vertical GaN PIN diodes are realized using CMOS-compatible contact materials. By using high quality and low resistive GaN bulk wafer (resistivity ~0.001 Ω.cm), the on-state resistance of the fabricated PIN here has been significantly reduced from our previous results [19]. Overall, the PIN diodes in this work show a record high figure-of-merit (V_{BR}^2/R_{on}) of 29.7 GW/cm^2.

2. Experiment details

Metal organic chemical vapor deposition (MOCVD) was used for the PIN epi structure growth in this work, and the PIN epi structure consists of 30-nm p^{++} GaN (Mg: 2×10^{20} cm^{-3}) contact layer, a 400-nm p-GaN (Mg: 1×10^{18} cm^{-3}) layer, a 20-μm n^- GaN drift region with a target Si doping concentration of 2.5×10^{16} cm^{-3}, and a 2-μm n^+ GaN buffer layer (Si: 2×10^{18} cm^{-3}) on a 350-μm thick free standing 2″ GaN substrate. The free standing 2” GaN substrate with a low resistivity is oxygen-doped and grown by ammonothermal method. Usually, HVPE is a common approach to fabricate highly doped GaN substrate, in which Si is used as n-type dopant. However, the highly n-type doped GaN substrate is difficult to be obtained. As increasing the flow rate of Si dopant precursor during HVPE growth, the free electron concentration cannot be further increased and kept in the range of $3–5 \times 10^{18}$cm^{-3}, since a large fraction of silicon donors are compensated by the gallium vacancies (as acceptors), which has a low formation energy barrier when the Fermi level is at the bottom of conduction band [20]. In addition, the GaN substrate with a high Si doping level of $5 \times 10^{18}–1 \times 10^{19}$cm^{-3} can be easily cracked during the growth, and is feasible to form SiN_x insulating particle. In this work, the highly conductive or highly doped n-type GaN substrate is grown by ammonothermal method, in which oxygen is used as the n-type dopant. As compared with Si dopant, oxygen is much easily to highly ($1 \times 10^{19}–1 \times 10^{20}$cm^{-3}) dope the GaN. The experiment was carried out in the ammonobasic solution in nickel-alloy autoclave, in which polycrystalline GaN was used as feedstock in the dissolution zone, and single crystal GaN was placed in the growth zone. Sodium and potassium amide were used as mineralizers to enhance the solubility of GaN. The temperature difference between the dissolution zone (~520 °C) and the growth zone (~570 °C) is ~50 °C, and growth rate is 80 μm/day. As compared to the PIN structure in the reported literature [19], a slightly higher doping concentration in drift layer is used to further reduce the drift resistance, since the drift resistance contributes into the major component of the total resistance, when the contact resistance is optimized. After PIN epi layer growth, thermal annealing in N_2 ambient at 750 °C for 30 min was carried to active the Mg acceptors in the p-layer. The p-type GaN layer has a hole concentration of 8.01×10^{16} cm^{-3} with a mobility of 29.2 cm^2/V·s at 25 °C, and the activation rate of Mg doped GaN is ~5-8%, as determined by Hall measurement. After PIN epi growth, the root-mean-square (rms) of GaN PIN epi surface is measured to be ~1 nm by atomic force microscopy (AFM) [Fig. 1 (a)], and the surface threading dislocation density is measured to be 3×10^5 cm^{-2} by cathodoluminescence (CL) [Fig. 1 (b)]. XRD (0002) and (10–12) rocking curves of GaN peak is shown in Fig. 3(c), in which the FWHM of (0002) and (10–12) planes is 21.67 and 37.08 arcsec, respectively, which are significantly lower than that of GaN-on-silicon and GaN-on-sapphire wafers (200–300 arcsec) [21].

After PIN active epi layer growth, pre-cleaning consisting of a 2-min acetone, a 3 min isopropanol degreasing step, and a 10-min dilute HCl (H_2O:HCl = 1:1) was carried out to remove native oxide. After metal stack of Al (70 nm)/Ti (30 nm) was deposited on the back-side of GaN wafer using an electron beam evaporator, anneal step under 800 °C for 30s was then performed to form the ohmic contacts. BCl_3/Cl_2 plasma etching (power: 300 W and pressure: 100 mTorr) was used to form the circular mesa structure with a diameter of 250 μm and depth of 900 nm. The Ni/Pt (30/130 nm) contact with a diameter of 170 μm was deposited as the anode electrode and alloyed at 550 °C for 5 min in N_2 ambient. Subsequently, a 200-nm SiO_2 by plasma-enhanced chemical vapor deposition (PECVD) was deposited to passivate the GaN surface. Before the field plate formation, a 1.5-μm spin-on-glass (SOG) film were coated on the devices and cured at 400 °C for 30 min. Contact holes were opened through SOG/SiO_2 layer by wet etching, and a Ti/Al/Ti/Al (15nm/150nm/15nm/150 nm) stack was deposited to form the field plate structure with a diameter of 300 μm. Complementary metal-oxide-semiconductor (CMOS) compatible contact materials (non-gold), such as Ti、Al、Ni etc., are used in this work. Fig. 1 (d) shows the side-view scanning electron microscopy (SEM) image of the fabricated vertical PIN diodes, and the schematic drawing of the fabricated devices is shown in Fig. 1 (e). In this work, the both forward and reverse current-voltage electrical characterizations were carried out using Agilent B1505A semiconductor analyzer and Cascade150 probe station. During the reverse recovery measurement, a pulse generator was applied to supply a periodic square-wave voltage signal from +7 V to - 30 V to the device under test, and the transient current variations were detected by a high speed current probe connecting to the Tektronix MDO 4104–3 oscilloscope to derive the reverse recovery wave form of PIN diodes.

3. Results and discussion

The forward current I_F (left-axis) and specific on-resistance R_{on} (right-axis) as a function of forward voltage V_F is plotted in Fig. 2 (a). In order not to highly overestimate the current density, the forward current in this work is normalized using the mesa area, which could overestimate the current density for a small device. It is more accurate to extract the current density by plotting current versus the device are, which could find out the portion of spreading current. The device shows on/off current ratio of ~1.3×10^7, if the on current and off current is defined as the current under forward voltage of 7 V, and 0 V, respectively. The turn-on or knee voltage (~2.5 V) is defined as the forward voltage when the current reaches 1A/cm^2. In Fig. 2 (a), the current rapidly increases when the forward voltage is larger than ~2.5 V, and the on-state resistance of ~0.31 mΩ.cm^2,

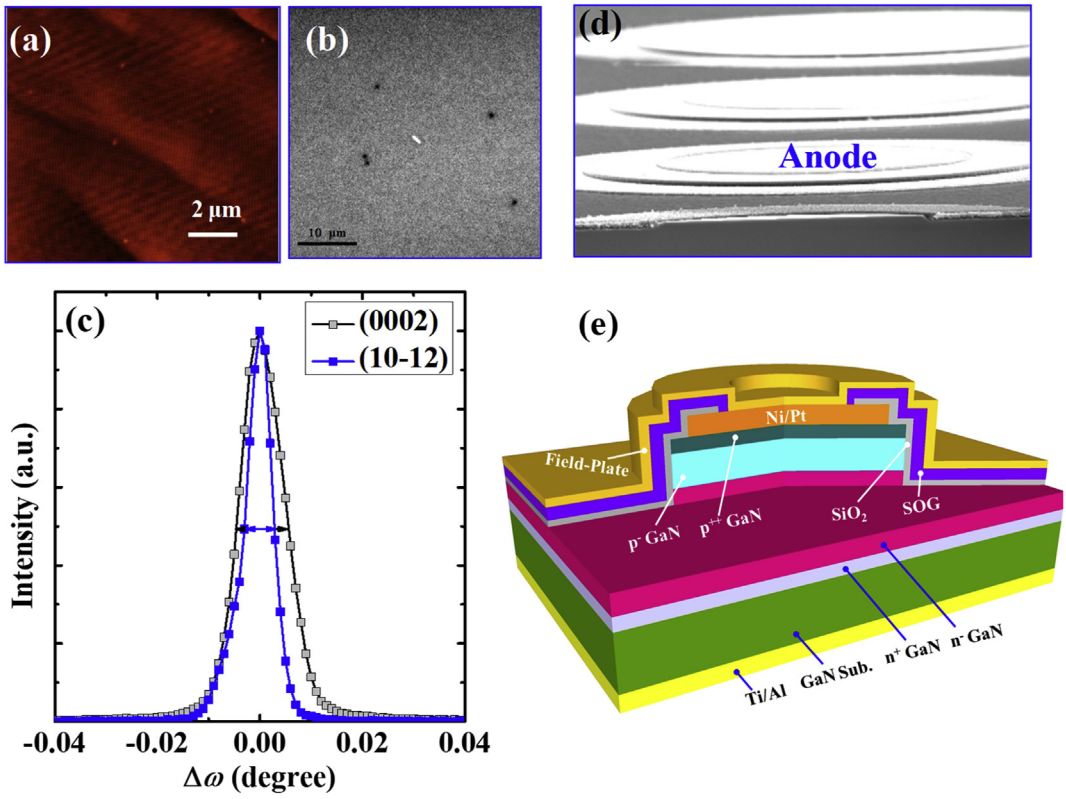

Fig. 1. AFM images of (a) GaN surface after PIN epi-layer growth; (b) cathodoluminescence (CL) image of GaN PIN epi surface.(c) Rocking curves of GaN (0002) and (10–12) peaks after epi; (d) Side-view SEM image of fabricated vertical GaN PIN diodes; (e) 3D drawing of the fabricated PIN devices.

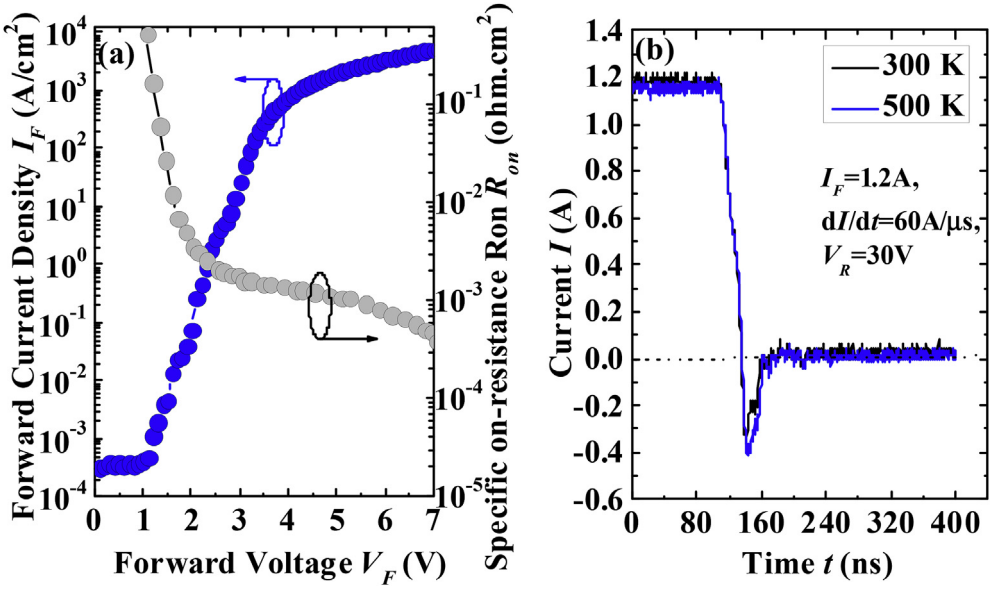

Fig. 2. (a) Forward current I_F and specific on-resistance R_{on} as a function of forward voltage V_F at 300 K. On-state resistance R_{on} of 0.31 mΩ cm^2 and on/off ratio of 1.3×10^7 are obtained. Forward current and specific on-resistance is normalized by the mesa area. (b) Reverse recovery characteristics of device under 300 K and 500 K, respectively.

which is mainly attributed by drift resistance, substrate resistance (~0.001 Ω.cm or 3.5×10^{-5} Ω cm^2), and contact resistance, is obtained at V_F of 7 V. Based on the transmission line measurement (TLM) structure, the contact resistance of Pt/Ni/p-GaN and Al/Ti/n-GaN is 1.06×10^{-5} Ω cm^2 and 4.0×10^{-6} Ω cm^2, respectively. The drift resistance can be obtained by subtract the substrate resistance and contact resistance from the total on-state resistance and calculated to be 2.6×10^{-4} Ω cm^2 (~84% of the total resistance). The drift resistance is attributed by both p-GaN and n-GaN, and proportional to $1/q(\mu_e N_D + \mu_h N_A)$, where μ_e or μ_h is the electron or hole mobility, N_D is the donor concentration in the n-GaN, and N_A is the acceptor concentration in the p-GaN. Based on the hole mobility of

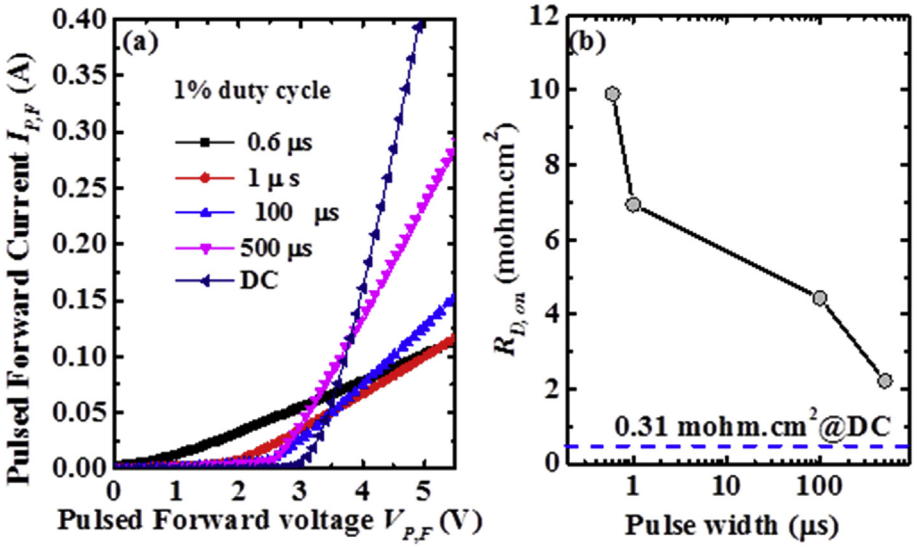

Fig. 3. (a) Forward current as a function of forward voltage under different pulse width with a fixed 1% duty cycle. (b) Dynamic on-state resistance $R_{D,on}$ as a function of pulse width with a fixed 1% duty cycle. On-state resistance is normalized by the mesa area.

29.2 $cm^2/V \cdot s$, the calculated resistance due to p-GaN layer is $1.14 \times 10^{-4}\,\Omega \cdot cm^2$ (~44% of the total drift resistance), thus the resistance of n-GaN layer can be obtained by subtracting the p-GaN resistance from the total drift resistance and estimated to be $1.46 \times 10^{-4}\,\Omega \cdot cm^2$. Based on the equation $I_F = I_o \exp(-qV_F/nkT)$, the minimum ideal factor n of the fabricated PIN diodes is ~2.3, where I_o is the reverse saturation current, q is the electronic charge, k is the Boltzmann constant, T is the measurement temperature. The ideality factor of 2.3 is obtained in the forward region of the device in this work, which is deviated from the ideal value of 1. Under the ideal condition, electrons and holes are recombinated through the band to band transition in the active region. However, the real case of PIN diodes usually has other processes, such as Shockley–Read recombination (SRH), in which the electron-hole recombination occurs through a localized state or deep traps, resulting in a large value of ideality factor.

Reverse recovery characteristics of the fabricated PIN diode are shown in Fig. 2 (b), and the PIN diode is switched from on-state to off-state with a switching speed (di/dt) of 60 A/μs. The reverse recovery time T_{rr} is defined as the sum of storage charge time in the depletion region (from zero reverse current to the maximum reverse current I_{RM}) and reverse current delay time (from the maximum reverse current I_{RM} to 0.1 I_{RM}), and reverse recovery charge Q_{rr} could be obtained by integrating the area under the reverse current I over the period of T_{rr}. With the increasing testing temperature from 300 K to 500 K, the reverse recovery time T_{rr} is increased from 22.8 ns to 24.0 ns, respectively, and the reverse recovery charge Q_{rr} is increased from 4.80 nC to 5.49 nC. When the PIN diode is switched from on-state to off-state, it takes time for the minority carrier to be extracted from the depletion process. As the T increases, the diffusion length of minority carrier hole (electron) in the n-region (p-region) of gallium nitride PIN diodes is increased, leading to more reverse recovery charge Q_{rr}, which results in longer time for the minority carrier to be extracted [22,23].

As shown in Fig. 3 (a), pulsed current under varied pulse width with a 1% duty cycle is plotted as a function of pulsed forward voltage. The pulsed current is decreased from 0.18 A to 0.08 A at pulsed voltage of 4.5 V, or the dynamic on-state resistance $R_{D,on}$ is increased from 2.22 mΩ.cm^2 to 9.90 mΩ.cm^2 [Fig. 3 (b)], as the pulse width decreasing from 500 μs to 0.6 μs. The increase of $R_{D,on}$ is related to the defects/traps with the PIN epi layer, and the traps could be non-ionized dopants with the epi layer. The on-state current is dominated by the series resistance, when the forward voltage passes the knee voltage. Depending on the MOCVD growth conditions, the density of defects/traps related to Mg or Si dopants can exceed ~10^{15} cm^{-3}, and the other two main deep level traps related to C、O impurities within PIN epi: 1.22 eV below the conduction band edge and 1.19 eV or 1.76 above the valence band edge [24]. These traps can affect device forward current under pulse mode due to pulse-dependent dynamic carrier ionization [25]. With the pulse width decreasing from 500 μs to 0.6 μs, the electrons trapped by the deep-level traps can accumulate in the active region, which further reduces the carrier mobility and increases the on-state resistance. More studies are needed to further verify the effect of traps within the GaN PIN epi layer.

During the high voltage measurement, the gallium nitride PIN diode is immersed in Fluorinert ambient to avoid the pre-mature breakdown. As shown in Fig. 4 (a), the device shows a hard breakdown voltage V_{BR} at 3.04 kV. The on-state resistance R_{on} of 0.31 mΩ cm^2 is extracted using the active region only. With R_{on} of 0.31 mΩ cm^2 and V_{BR} of 3.04 kV, this device achieves a power device figure-of-merit (FOM) V_{BR}^2/R_{on} of 29.7 GW/cm^2. It is noted that Baliga's FOM is based upon the assumption, which is that the power losses are solely due to the power dissipation in the on-state by current flow through the on-resistance of the unipolar power device. In this work, PIN diode is a bipolar device, in which both electrons and holes can contribute the forward current, or the drift resistance is attributed by both p-GaN and n-GaN. However, p-GaN layer in this work has a lower hole mobility (~29.2 $cm^2/V \cdot s$) and thinner thickness (430 nm), as compared with n-GaN layer (electron mobility of 1200 $cm^2/V \cdot s$ and thickness of 22 μm). Therefore, the vertical GaN PIN diode in this work can be approximately treated as a unipolar device. Fig. 4 (b) shows V_{BR} versus R_{on} obtained in this work and other state-of-the-art vertical gallium nitride PIN diodes. As compared to the reported ones, the device fabricated in this work using CMOS-compatible contact materials has achieved the best figure-of-merit (FOM) V_{BR}^2/R_{on} of 29.7 GW/cm^2. As compared with the same breakdown voltage, the PIN device in this work shows lower on-state resistance. Fig. 5 (a) shows the electrical field contour of the vertical PIN device without a field plate under 3000 V reverse bias, and the maximum electrical field is along the mesa edge in the corner. With incorporating the metal field plate in

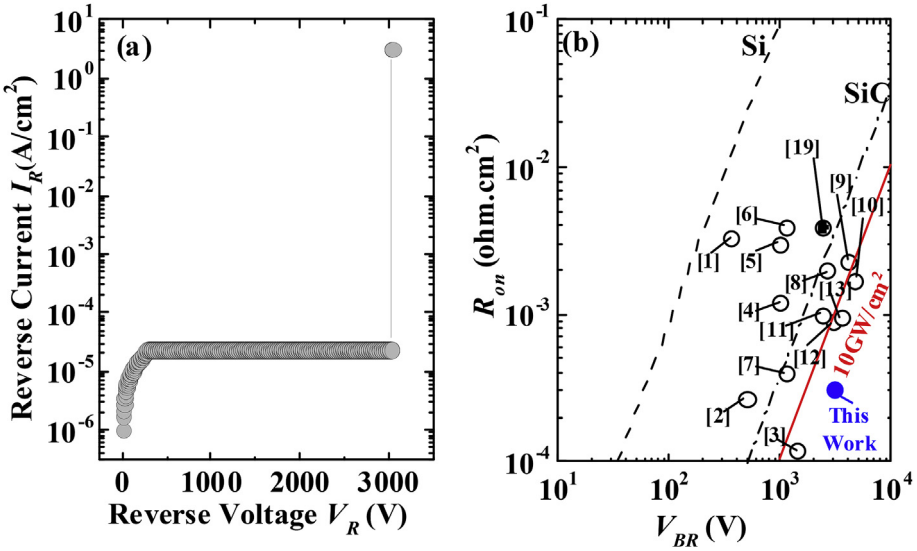

Fig. 4. (a) Reversed current as a function of reversed voltage. Inset shows the cumulative distribution of V_{BR}. (b) Benchmarking of on-state resistance R_{ON} versus breakdown voltage V_{BR} for the published ones. (Solid symbol: Au-free; Open symbol: with Au).

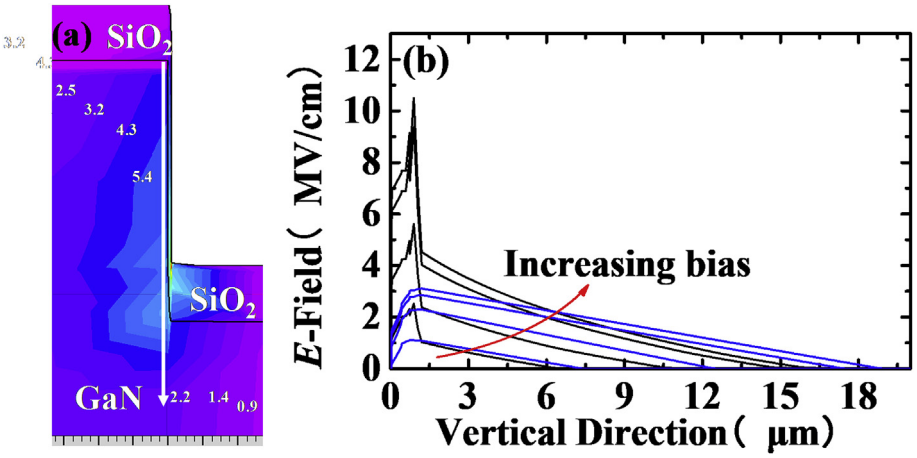

Fig. 5. (a) Illustration of the electrical field distribution of the vertical PIN diode without field plate under 3000 V reverse bias, and the maximum electrical filed is along the vertical mesa edge near the lower mesa corner. (b) Electrical field (*E*-field) in the vertical direction with 1 nm away from the mesa edge, as indicated in (a), is plotted for the device with and without field plate structure. The reverse biases are 500 V, 1500 V, 3000 V, and 4000 V.

the vertical PIN diode, the maximum electrical field peak or electrical field spark can be significantly reduced. Fig. 5(b) shows the electrical field (*E*-field) distribution under various reverse biases (500 V, 1500 V, 3000 V, and 4000 V) in the vertical direction with 1 nm away from the mesa edge, as indicated in Figure (a). With incorporating the metal field plate structure, the maximum electrical peak or spark will be significantly reduced. For example, the peak electrical field of the device with field plate structure is reduced from 9.4 MV/cm to 3.2 MV/cm under 3000 V reverse bias.

4. Conclusion

In summary, vertical GaN-on-GaN PIN diodes with a record high figure-of-merit (V_{BR}^2/R_{on}) of 29.7 GW/cm^2 have been demonstrated in this work. Due to the low substrate resistivity, low contact resistance, and high quality of GaN drift layer, low on-state resistance R_{on} of 0.31 mΩ cm^2 is obtained. With integrating of the metal filed plate structure in the vertical device, the peak electrical field along the GaN mesa edge can be significantly reduced, thus leading to a high breakdown voltage V_{BR} of 3.04 kV. Both static and switching electrical characterization have been executed to evaluate the performance of vertical GaN-on-GaN PIN diodes with gold-free process, which paves the way of high performance GaN diodes in the commercial applications.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at https://doi.org/10.1016/j.jallcom.2019.07.021.

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