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All-optical logic gates using dielectric-loaded waveguides with quasi-rhombus metasurfaces

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Nanostructure and nanoantenna-based all-optical (AO) devices have attracted significant research interests in recent years due to their small size, high information capacity, ultrafast processing, low power consumption, and overall practicality. Here, in this Letter, we propose a novel metasurface having quasi-rhombus-shaped antennas to modulate optical modes in a dielectric-loaded waveguide for the realization of a complete family of logic gates including NOT, AND, OR, XOR, NAND, NOR, and XNOR. These logic operations are realized using destructive and constructive interferences between the input optical signals. The high contrast ratios of about 33.39, 27.69, and 33.11 dB are achieved for the NAND, NOR, and XNOR logic gates, respectively, with the speed as high as 108 Gb/s. © 2020 Optical Society of America

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Recently, nanostructure and nanoantenna-based all-optical (AO) devices have played important roles in integrated photonic circuits (IPCs) due to their compact size, high information capacity, ultrafast processing, low power consumption, and overall practicality. However, the inherent optical diffraction limit provides a fundamental limit for the reduction in the size of optical components in IPCs to compete with their electronic analog. Significant research efforts have been paid to scale down photonic devices [1,2] and ease of their integration with the mature Si microelectronics [3]. Indeed, the ultrafast performance of AO logic gates using silver nanowire network [4,5], plasmonic slot waveguides [6,7], dielectric-loaded waveguides (DLWs) [8], metal structures [9], silicon hybrid plasmonic waveguides [10], and semiconductor amplifiers [11] have been reported. Recently, metasurfaces have attracted strong interests in nanophotonic device development due to their unique electromagnetic material response [12,–15]. Owing to their unique features including compactness, low loss, and low-temperature dependence, DLWs are also used in the design and fabrication of passive photonic devices [16–18].

Metasurfaces can be integrated with the DLWs for the realization of a complete family of basic Boolean functions and other PIC components [18]. However, most of the research on AO logic gates for PICs are centered to the communication wavelength; therefore, handheld optical devices, operating at the communication wavelength, are susceptible to interception and interference. On the other hand, visible light communications (VLCs) can be used for highly secured indoor communication at spaces sensitive to the interference from communication wavelength. The recent advancements and advantages of VLCs over the conventional long wavelength communication motivated us to design AO logic gates in the visible spectral region.

Following our previous work [19], here, we designed another quasi-rhombus metasurface (QRM) with silver (Ag) nanorods antennas patterned directly at the top surface of the DLW [Fig. 1(a)]. Owing to the high transparency and high sensitivity of Al and Al_2O_3 in the UV-visible spectra region along with their CMOS compatibility, and ease of integration with the mature Si microelectronics, the DLW is designed with 200 nm thick alumina (Al_2O_3) ridge on the surface of 100 nm thin aluminum film on a glass substrate. A periodic array of silver nanorods forms a gradient metasurface. Figure 1(b) shows the spectral variations in the effective index and the corresponding loss in the DLW of 1.05 μm width. The effective wave vector effectively controls waveguide modes through strong and consecutive scattering processes at the surface of antenna array [19,20]. Thus, compared to the bare DLW [Fig. 1(c)], the DLW with metasurface [Figs. 1(d) and 1(e)] demonstrates the conversion of a fundamental TM mode into a higher-order mode where the higher-order TM modes are periodically getting self-imaged.

The finite-difference-time-domain (FDTD) simulation was performed with the convolutional perfectly matched layer (PML) as an absorbing boundary condition. The structure is excited by a TM polarized wave at 471 nm wavelength (see Fig. 1). The silver permittivity and Al_2O_3 refractive index values were obtained from Johnson and Christy [21] and Malitson and Dodge [22], respectively. Intensity monitors were used to measure the intensity values at the input and output ports and in the *x-y* and *x-z* planes of the waveguides and logic gates. The
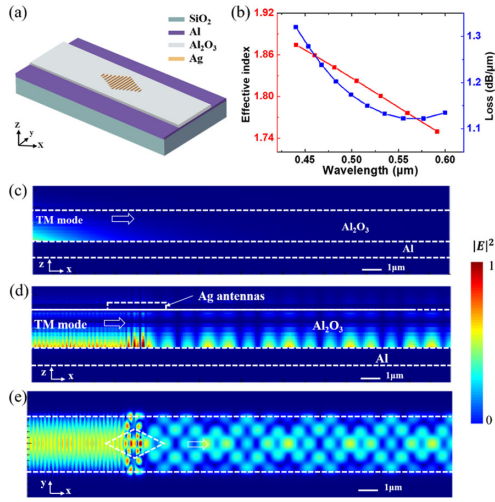
Fig. 1. (a) Schematic illustration of a DLW with a QRM. (b) Effective index and corresponding loss as a function of wavelength. Spatial distribution of power in DLW waveguides: (c) without, and (d) and (e) with a QRM in x-z and x-y planes, respectively.
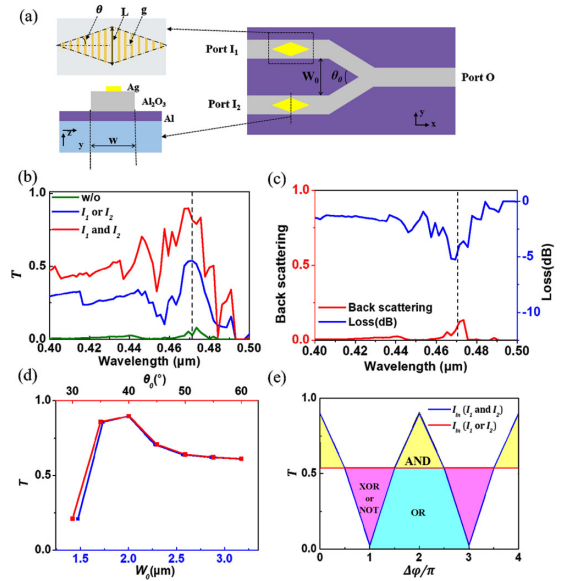

Fig. 2. (a) Schematic of two input port logic gates based on DLW waveguide and QRMs. (b) Normalized spectral transmittance of the optimized Y-shaped DLWs. (c) Corresponding spectral backscattering and loss. (d) Optimization of W_0 and θ_0 at 470 nm wavelength. (e) Normalized transmittance as a function of phase difference between two input arms.

ratio of the output to input light intensities ($T = |E_o|^2/|E_i|^2$, where E_o and E_i are the electric field intensities at output and input, respectively) was used to measure the transmittance and hence response at the output of the logic gates.

To implement the AO logic gates, a NOT gate is essential. Utilizing our previous experiences [18,19], we optimized a set of parameters for silver nanoantennas of QRM to optimize transmission for a long-distance propagation of the high-order mode through the DLW (width 1.06 μm). The length of the largest nanorod (L), gap (g), and angle (θ) for the QRM are 600 nm, $g = 250$ nm, and $\theta = 6.98°$, respectively. For the bare DLW, it is difficult to change the output state because of its low transmission [Fig. 1(c)]. However, due to the presence of QRM on the surface of DLW, the high-order TM modes can propagate for a long-distance [Figs. 1(d) and 1(e)]. Owing to the uniqueness of the gradient metasurface, the incident wave needs to satisfy the phase-matching conditions to optimize the transmission. When the phase of the incident wave is changed to mismatch with the gradient metasurface, the incident wave gets scattered resulting in the reduced transmission. This strategy is utilized here to design AO logic gates. We first set a threshold transmission value (T_{th}). The state can be in logic "1" when $T > T_{th}$ otherwise in the state "0". Thus, the NOT operations can be realized by changing the phase of the input signal.

The AND, OR, and XOR logic gates are designed using three DLWs in the Y shape, as shown in Fig. 2(a). In the device, two input ports, marked as I_1 and I_2, and one output port, marked as O, are used. The QRM is set on the top of the both input ports. The input beams propagating through the Y-shaped waveguide face a strong loss due to backscattering at the junction. To overcome the loss at the junction, a small angle (θ_0) between the two input arms, as shown in Fig. 2(a), is necessary. However, very small θ_0 would lead to the cross talk between the two input beams. To avoid an unintended cross talk, we optimized the angle and distance between the two input arms as 40° and 2 μm, respectively [Fig. 2(d)]. Figure 2(b) shows the normalized spectral transmission, defined as $T = I_{out}/I_{in}$, where $I_{out} = |E_o|^2$ is the intensity at the port O and $I_{in} = I_1 + I_2$ is the sum of the intensities at two input ports. The green line represents the T

for the bare DLW. The blue and red lines represent the T curves for the QRM functionalized DLW with light entering to only one of the input ports (I_1 or I_2) and both inputs (I_1 and I_2), respectively. As compared to the bare Y-shaped waveguide, the integration of the QRM improved transmission by an order of magnitude. The normalized T with the two inputs is much higher than the one input possibly due to the constructive interference between two input incident waves after the QRM. We can see that T from the bare, as well as the QRM functionalized DLWs, has peaks around 471 nm. The spectral backscattering and spectral loss for the optimized Y-shaped geometry are also shown in Fig. 2(c).

The phases of the input I_1 and I_2 are defined as φ_1 and φ_2, respectively, and the phase difference between the two input signals is defined as $\Delta\varphi = |\varphi_1 - \varphi_2|$. The two input light signals have the same intensity and wavelength. Figure 2(e) shows the variation in the T of the Y-shaped DLWs with $\Delta\varphi$ for single (red line) and two (blue line) input signals at 471 nm wavelength. For the blue line, the minimum ($T_{min} = 0.033$) and the maximum ($T_{max} = 0.8$) T values correspond to the $\Delta\varphi = (2n + 1)\pi$ and $2n\pi$ ($n = 0, 1, 2, \ldots$), respectively. The Boolean function can be controlled by the threshold transmission intensity (T_{th}). When $T_{out} > T_{th}$, the output value is at logic state "1" while "0" otherwise. In Fig. 2(e), we chose 0.1 as the T_{th} for $\Delta\varphi = \pi$ and 2π, to realize XOR (or NOT) and OR operations (pink and blue area). However, we also chose 0.1 as T_{th} at $\Delta\varphi = 2\pi$ to realize AND logic operation (yellow area). Thus, different optical logic functions, AND, OR, and XOR, can be realized at different values of $\Delta\varphi$ by defining corresponding threshold values.

The simulated field distribution for all optical logic functions is shown in Fig. 3, and the results are summarized in Table 1. For OR operation, In Fig. 3(a-1), $I_1 = 1$, $I_2 = 0$, the amplitude value of the output signal is 0.553 ($> P_{th}$), resulting in
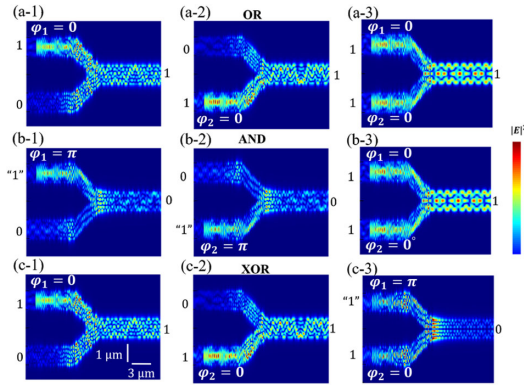
Fig. 3. Distribution of field intensity for OR gates, AND gates, and XOR gates. The input signals with $\varphi = \pi$ are "1".
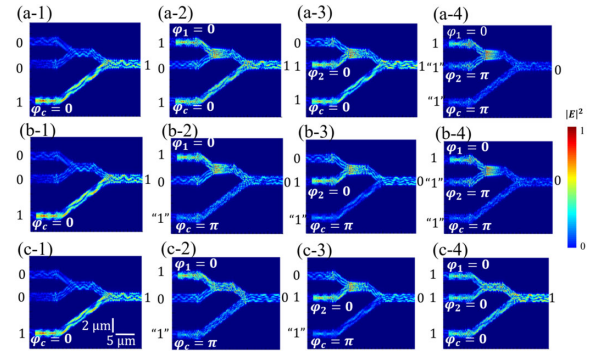

Fig. 4. Distribution of electric field intensity for three input ports gates: (a) NAND, (b) NOR, and (c) XNOR gates. The input signals with $\varphi = 0$ are 1. The input signals with $\varphi = \pi$ are "1".

Table 1. Operating Principle of the AND, OR, and XOR Gates

Logic Gates	Amplitude of Input Field		Amplitude of Output Field	Logic Output	Intensity Contrast Ratio (dB)
	Port I_1	Port I_2	Port O		
I_1 OR	0	0	0	0	28.676
I_2	1	0	0.553	1	
	0	1	0.548	1	
	1	1	0.896	1	
I_1 AND	0	0	0	0	28.676
I_2	1	0	0.029	0	
	0	1	0.026	0	
	1	1	0.896	1	
I_1 XOR	0	0	0	0	24.406
I_2	1	0	0.553	1	
	0	1	0.548	1	
	1	1	0.033	0	

Table 2. Operating Principle of the NAND, NOR, and XNOR Gates

Logic Gates	Amplitude of Input Field			Amplitude of Output Field	Logic Output	Intensity Contrast Ratio (dB)
	Port I_1	Port I_2	Port C	Port O		
I_1 NAND	0	0	1	0.509	1	33.390
I_2	1	0	1	0.802	1	
	0	1	1	0.841	1	
	1	1	1	0.018	0	
I_1 NOR	0	0	1	0.509	1	27.690
I_2	1	0	1	0.020	0	
	0	1	1	0.021	0	
	1	1	1	0.018	0	
I_1 XNOR	0	0	1	0.509	1	33.110
I_2	1	0	1	0.020	0	
	0	1	1	0.021	0	
	1	1	1	0.950	1	

$O = 1$. Similarly, $I_1 = 0$, $I_2 = 1$ [Fig. 3(a-2)] can be accomplished. For $I_1 = 1$, $I_2 = 1$ [Fig. 3(a-3)], the amplitude value of the output signal is 0.896 ($> T_{th}$) because of the constructive interference in the output port, which corresponds to the logic state of "1" OR "1" = "1". To achieve AND logic function, the simulated fields are shown in Figs. 3(b-1)–3(b-3), where the T values at the output ports are 0.029 ($< T_{th}$), 0.026 ($< T_{th}$) and 0.896 ($> T_{th}$). In Figs. 3(b-1) and 3(b-2), the phase of the incident waveguide mode is π, and the incident wave propagates against the phase gradient $d\Phi/dr$ (k_{eff}) wave vector. The incident waveguide mode is converted into the surface wave that cannot propagate to a long distance due to the gradient metasurface.

To realize the XOR logic function, the simulated field distributions are shown in Figs. 3(c-1)–3(c-3), where the T values at the output ports are 0.553, 0.548, and 0.033. The equal amplitudes of both input signals [Fig. 3(c-3)] with $\Delta \varphi = \pi$ cause destructive interference at the port O to result in the intensity value 0.033 ($< P_{th}$) to get logic "0". The intensity contrast ratio of XOR logic functions between the output logic "1" and "0" is 24.406 dB, which is calculated from $10 \log(I_1/I_0)$, where I_1 and I_0 are the intensities ($|E|^2$) for logic "1" and logic "0" at port O, respectively.

To illustrate the invert logic gates, NAND, NOR, and XNOR gates, three input waveguides, two input ports of the Y-shaped DLWs and a control input port C, are required. The distance between input ports I_2 and C is optimized to 4 μm ($2W_0$) to achieve a destructive or constructive interference, at the output waveguide, for the TM modes with $\Delta \varphi = (2n + 1)\pi$ or $\Delta \varphi = 2n\pi$ propagating through I_1 (or I_2) and C waveguides. The phase of the control input C is defined as φ_c.

The simulated field distribution of the NAND, NOR, and XNOR gates is shown in Fig. 4, and the simulated results are summarized in Table 2. For the NAND operations [Figs. 4(a-1)–4(a-4)], when both inputs (I_1 and I_2) are zero [Fig. 4(a-1)], the control signal C with $\varphi_c = 0$ passes through the structure, resulting in the T value 0.509 leading to logic "1". Since the phase of the control signal is maintained at $\varphi_c = 0$, therefore, the TM mode with $\varphi = 0$ passing through one of the two input ports I_1 or $2I_2$ ($I_1 = 1$, $I_2 = 0$ [Fig. 4(a-2)] or $I_1 = 0$, $I_2 = 1$ [Fig. 4(a-3)] results in $\Delta \varphi = 0$ between control and input signal, leading to the constructive interference at the output port O with $T = 0.8$ ($> T_{th}$) i.e., logic "1". However, in Fig. 4(a-4), when two input ports ($I_1 = I_2 = 1$) with $\Delta \varphi = \pi$ and the control port C with $\varphi_c = \pi$ are excited simultaneously,
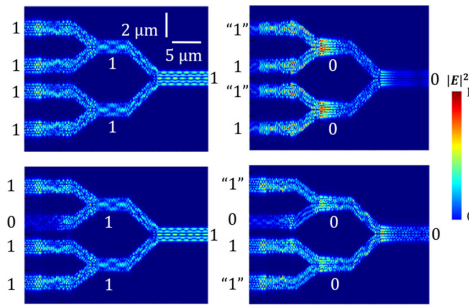
Fig. 5. Left, cascading two OR and, right, two AND logic gates.

the transmission at the output port becomes 0.018 ($< P_{th}$), resulting in the logic "0". The contrast ratio between the ON and OFF states is about 33.39 dB. For the NOR operations [Figs. 4(b-1)–4(b-4)], when one of the input ports is at logic state 1($I_1 = 1$, $I_2 = 0$ or $I_1 = 0$, $I_2 = 1$) with 0 phases for both inputs and the phase of the control signal C is π [Figs. 4(b-2) and 4(b-3)], the transmission at the output port O is about 0.02 ($< T_{th}$), leading to the logic 0 at port O due to the destructive interference between the control port C and the input port I_1 (or I_2). If setting 0.033 for the threshold value, the contrast ratio is about 27.69 dB. Similarly, for XNOR operations, $\varphi = 0$ at two input ports, I_1 and I_2, and the control port C [Fig. 4(c-4)] results in a constructive interference between three input ports to make the transmission at the output port O as high as 0.95 with the contrast ratio $\sim$ 33.11 dB. Cascadability is an important characteristic of logic gates; therefore, the proposed design must demonstrate cascadability. Figure 5 shows cascading of two OR logic gates (left), and two AND logic gates (right). Nyquist theorem is used herein to calculate the maximum data rate, i.e., data rate $= 2B \log 2M$ [23], where B is the optical bandwidth and M is the number of the signal levels. Thus, the number of bits transferred using the proposed structure at 471 nm wavelength and for four signal levels (00, 01, 10, 11) is 108 Gb/s.

The performance of the proposed logic gates in comparison with the previously reported structures is presented in Table 3. The functionalization of the DLW with metasurface structure in the proposed structure resulted in the contrast ratio higher than

24 dB. The field caused by TM higher-order modes is generated by the multimode interference (MMI) of QRM. The logic state of input ports depends on the polarization of the incident wave.

In summary, the effects of the QRMs on the DLWs have been studied to realize AO logic gate operations. The Y-shaped DLWs with QRM are proposed for the realization of high-performance NOT, AND, OR, XOR, NAND, NOR, and XNOR logic gates. The operational principles of these gates are based on the constructive and destructive interferences caused by the difference in the phase of the input signals. The high contrast ratios of about 33.39, 27.69, and 33.11 dB are achieved for the NAND, NOR, and XNOR logic gates, respectively, with the speed as high as 108 Gb/s.

Disclosures. The authors declare no conflicts of interest.

Table 3. Comparison between Our Work and Previous Work

Structure	Logic Functions	Operation Wavelength (nm)	Contrast Ratio (dB)
Periodic Si rods [24]	OR, NAND, NOR, NOT	1550	8.8–15.6
MMI Waveguides [25]	XOR, XNOR, NAND, OR	1530–1565	25–28.6
Gold disk-array [26]	XOR, NAND	451.8	26, 24
Metal waveguide [27]	OR, NOT, XOR	632.8	9.3–13.98
Our works	AND, XOR, NAND, OR, NOR, NOT, XNOR	471	24.4–33.4

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