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320 Gb/s all-optical logic operations based on two-photon absorption in carrier reservoir semiconductor optical amplifiers

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ABSTRACT

When a train of optical pulses is injected, two-photon absorption (TPA)-induced pumping results in significant and fast gain and phase shifts in the carrier reservoir semiconductor optical amplifier (CR-SOA). Therefore, in this work, the effect of TPA on all-optical (AO) exclusive-OR (XOR), AND, NOT-OR (NOR), OR, NOT-AND (NAND), and exclusive-NOR (XNOR) logic operations using CR-SOAs is theoretically implemented for the first time at 320 Gb/s. The XOR, AND, NOR, NAND, and XNOR logic gates are implemented using the Mach-Zehnder interferometer, which has two symmetrical CR-SOAs in each of its two arms, whereas the OR logic gate is produced by combining a CR-SOA with a delayed interferometer. The quality factor (QF) and the associated bit error rate (BER) metrics are employed to evaluate the operations' performance. The obtained simulation results indicate that when exploiting TPA in CR-SOAs the target Boolean functions can be executed with QF and BER that are more than acceptable than without TPA at a high speed up to 320 Gb/s. Various circuits of enhanced logic functionality, such as AO half-adder, latches, comparator, half-subtractor, and encoder can be implemented by combing the presented AO gates and hence exploiting the ultrafast TPA-induced gain and phase changes in CR-SOAs. Furthermore, the potential of CR-SOAs as nonlinear elements is systematically and thoroughly established for a wide suite of AO logic operations.

1. Introduction

The semiconductor optical amplifier (SOA) is a well-established technique for implementing all-optical (AO) logic gates [1–3] and related applications [4–6] owing to its small size, high nonlinearity, and simplicity of integration with other photonic elements. On the turning side, it's the SOAs response recovers slowly after it has been intensely perturbed, which is a fact that obstructs SOAs to operate at speeds exceeding 100 Gb/s [7]. The two-photon absorption (TPA) nonlinear phenomenon, on the other hand, can be leveraged to bypass the physical limits of traditional SOAs by inducing large and ultrafast gain and phase variations that can be used for AO logic purposes. TPA has been used in SOAs to increase the speed of logic operations up to 250 Gb/s, as shown numerically in [8–12].

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The carrier reservoir SOA (CR-SOA), on the other hand, relies on a similar operation principle as that for a quantum dot (QD)-SOA, in which the wetting layer (WL) serves as a CR layer [13]. The input pulse depletes the carriers in the QD ground state in QD-SOA, and they are restored by rapid carrier transfer from the WL. More carriers are delivered in the WL when the injected current density is increased, resulting in a faster response time [7]. In CR-SOA, the CR provides carriers to the active region with a transition time similar to QD-SOA. The gain dynamics are dominated by this ultrafast transition, hence the CR-SOA exhibits a similarly fast temporal gain and phase response as the QD-SOA. The inversion factor of QD-SOAs is significantly reduced due to the limited number of possible states in QDs, allowing for even faster operation. In addition, uniform QDs are less technologically developed and more difficult to produce, thereby compromising QD-SOAs overall practicality [14]. This effectively implies that creating CR layers using current semiconductor processing techniques may be more practicable for CR-SOAs, and hence may be preferable in terms of cost, complexity, and general usability. In this context, the performance of AO logic gates using CR-SOAs has recently been investigated [14–17]. In this study, the physical benefits of TPA have been combined with those of CR-SOAs to theoretically implement AO exclusive-OR (XOR), AND, NOT-OR (NOR), OR, NOT-AND (NAND), and exclusive-NOR (XNOR) XOR logic gates at 320 Gb/s. The performance of the studied logic gates has never been investigated before utilizing CR-SOAs with induced TPA at 320 Gb/s, to the best of the authors' knowledge. The Mach-Zehnder interferometer (MZI), which has two symmetrical CR-SOAs arranged in its two arms, is used to implement the XOR, AND, NOR, NAND, and XNOR logic gates, while the OR logic gate is built by combining a CR-SOA with a delayed interferometer (DI). The MZI is a well-established choice for AO switching owing to its appealing properties such as simple structure, high stability, efficient operation, and, overall, practicality [9]. The DI, on the other hand, provides a phase window whose duration is controlled by the DI's shorter delay, which is beneficial to the output signal's quality [18]. The gates' performance was evaluated using the quality factor (QF) and the accompanying bit error rate (BER). The results were obtained utilizing CR-SOAs at 320 Gb/s with TPA and without TPA for performance comparison. These results show that exploiting TPA in CR-SOA allows the target AO logic gates to operate at 320 Gb/s with more than acceptable QF and BER than when TPA is idle.

The main research contribution of this study of the performance of the considered AO logic gates, which has not been previously done using CR-SOAs with induced TPA at 320 Gb/s. As these gates are fundamental in numerous combinational and sequential circuits and subsequent applications, the outcome of this study can contribute to the design and implementation of these circuits, which are necessary for the development and realization of lightwave systems and networks that fully exploit the advantages of AO solutions for efficiently satisfying users' demanding needs. Moreover, another important contribution is the establishment of CR-SOAs technology, whose potential had so far not systematically and thoroughly been investigated and assessed. By showing that CR-SOAs are indeed capable of supporting a wide suite of nonlinear switching operations, new research perspectives can be opened in the relevant field and an additional tool can be made available in the effort to overcome the limitations of other technologies that have been explored for the same purpose.

2. CR-SOA model

The CR layer has a greater bandgap than the active region (AR) layer in CR-SOA. Carriers in AR and CR begin to fill the available states when an injection current is applied. At low current, the AR has a larger carrier density than the CR. As the injection current is raised, the CR accumulates enough carriers to serve as a reservoir of supplied carriers. The incident photons are driven into the AR by the stimulation emission mechanism and collide with electrons, creating photons. The heavily filled CR quickly replaces the carriers depleted in the AR by an intense signal in the active area. Transitions from the CR to the AR can occur in a few picoseconds [7], accelerating the CR-SOA gain and phase response. The TPA-induced optical pumping provides extra carriers in addition to those provided by electrical pumping [3], resulting in a higher rate of carrier capture into the CR-SOA and accordingly in a significant improvement of its carrier recovery dynamics, which is reflected on the switching configuration in which the CR-SOA is employed as nonlinear element. The time-dependent gain differential equations for each CR-SOA are as follows, accounting for both intraband nonlinear effects of carrier heating (CH) and spectral hole burning (SHB), i.e. [13–17]:

$$\frac{dh_{AR}(t)}{dt} = \frac{h_{CR}(t)-h_{AR}(t)}{\tau_t(1+\eta)} + \frac{\eta h_0}{\tau_c(1+\eta)} - \frac{h_{AR}(t)}{\tau_c} - \left(exp\left[h_{AR}(t) + h_{CH}(t) + h_{SHB}(t)\right] - 1\right)\frac{P_{in,\ CR-SOA}(t)}{E_{sat}} \tag{1}$$

$$\frac{dh_{CR}(t)}{dt} = -\frac{\eta(h_{CR}(t)-h_{AR}(t)}{\tau_t(1+\eta)} + \frac{h_0-h_{CR}(t)}{\tau_c(1+\eta)} - \frac{h_{CR}(t)}{\tau_c} \tag{2}$$

$$\frac{dh_{CH}(t)}{dt} = -\frac{h_{CH}(t)}{\tau_{CH}} - \frac{\varepsilon_{CH}}{\tau_{CH}}\left(exp\left[h_{AR}(t)+h_{CH}(t) + h_{SHB}(t)\right] - 1\right)P_{in,CR-SOA}(t) \tag{3}$$

$$\frac{dh_{SHB}(t)}{dt} = -\frac{h_{SHB}(t)}{\tau_{SHB}} - \frac{\varepsilon_{SHB}}{\tau_{SHB}}\left(exp\left[h_{AR}(t) + h_{CH}(t) + h_{SHB}(t)\right] - 1\right)P_{in,\ CR-SOA}(t) - \frac{dh_{AR}(t)}{dt} - \frac{dh_{CH}(t)}{dt} \tag{4}$$

where the CR-SOA's gain integrated over its length for the carrier recombination between AR and CR, CH, and SHB is represented by functions h_{AR}, h_{CR}, h_{CH}, and h_{SHB}, respectively. $\eta = N_{AR}/N_{CR}$ [13–17] is the population inversion factor, $h_0 = \ln[G_0]$ is the unsaturated power gain given by $G_0 = \alpha\Gamma(I\tau_c/eV - N_{tr})L$ [7], and $E_{sat} = P_{sat}\,\tau_c = wd\hbar\omega_0/\alpha\Gamma$ [7] is the saturation energy. $P_{in,\ CR\text{-}SOA}(t)$ is the input signal power comprising of Gaussian-shaped return-to-zero pulses, i.e. [14–17]:

Table 1
Default simulation parameters [1–22].

Symbol	Definition	Value	Unit
E_0	Pulse energy	0.2	pJ
τ_{FWHM}	Pulse width	0.5	ps
T	Bit period	3.125	ps
N	PRBS length	127	-
λ_A	Wavelength of A	1549.2	nm
λ_B	Wavelength of B	1535	nm
λ_{CW}	Wavelength of CW	1550	nm
λ_{Clk}	Wavelength of Clk	1555	nm
$\Delta\tau$	Time delay (AND operation)	0.25	ps
$\Delta\tau_{DI}$	DI delay time (OR operation)	0.2	ps
$\Delta\Phi_{DI}$	DI phase bias (OR operation)	π	rad
I	Injection current	200	mA
P_{sat}	Saturation power	30	mW
τ_c	Carrier lifetime	200	ps
τ_t	Transition lifetime from CR to AR	5	ps
η	population inversion factor	0.3	-
α	α-factor	5	-
α_{CH}	CH linewidth enhancement factor	1	-
α_{SHB}	SHB linewidth enhancement factor	0	-
α_{TPA}	TPA linewidth enhancement factor	-4	-
β	TPA coefficient	20	cm/GW
ε_{CH}	CH nonlinear gain suppression factor	0.2	W^{-1}
ε_{SHB}	SHB nonlinear gain suppression factor	0.2	W^{-1}
τ_{CH}	Temperature relaxation rate	0.3	ps
τ_{SHB}	Carrier-carrier scattering rate	0.1	ps
Γ	Confinement factor	0.3	-
ɑ	Differential gain	10^{-16}	cm^2
N_{tr}	Transparency carrier density	10^{18}	cm^{-3}
L	AR length	500	μm
d	AR thickness	0.3	μm
w	AR width	3	μm
G_0	Unsaturated power gain	30	dB
ħ	Reduced Planck's constant	1.05×10^{-34}	J.s

$$P_{A,\,B,\,Clk}(t) \equiv P_{in,\ CR-SOA}(t) = \sum_{n=1}^{N} a_{n(A,\,B,\,Clk)} \frac{2\sqrt{\ln[2]}\ \ E_0}{\sqrt{\pi}\ \ \tau_{FWHM}} \ \ exp\left[-\frac{4\ln[2]\ \ (t\ -\ n\,T)^2}{\tau_{FWHM}^2}\right] \tag{5}$$

where $\alpha_{n(A,\,B,\,Clk)}$ is the n-th pulse either in data streams A, B which are pseudorandom binary sequences (PRBS) of length $N = 2^7$-1, or clock signal (Clk). The definitions of all default parameters are listed in Table 1 [1–22].

The CR-SOA's overall gain is then calculated as follows [14–17]:

$$G_{CR-SOA_i}(t) \ = \ exp\ [h_{AR}(t)\ +\ h_{CH}(t)\ +\ h_{SHB}(t)\,], \qquad i = 1,2,3,4 \tag{6}$$

The CR-SOA's induced phase change is given by [14–17]:

$$\Phi_{CR-SOA_i}(t) \ = \ -\ 0.5\ (\alpha\, h_{AR}(t)\ +\ \alpha_{CH}\, h_{CH}(t)\ +\ \alpha_{SHB}\, h_{SHB}(t)), \qquad i = 1,2,3,4 \tag{7}$$

where the normal linewidth enhancement factor is α (i.e. α-factor) and the linewidth enhancement factors associated with CH and SHB are α_{CH} and $\alpha_{SHB,}$ respectively.

The TPA of a high-intensity pump beam alters the carriers' quantity in the AR of the CR-SOA, causing a phase shift in a low-intensity probe beam passing through the amplifier. The magnitude of the phase change of the TPA effect is given by [7–12]:

$$\Phi_{TPA}(t) = \ -\ 0.5\beta\alpha_{TPA} L\, S(t) \tag{8}$$

where β is the TPA coefficient, α_{TPA} is the TPA linewidth enhancement factor, and S(t) is the light intensity. TPA-induced phase and gain changes are in the opposite direction to the phase change due to CR-SOA gain, as seen by the negative sign in Eq. (8). The overall phase of the CR-SOA, including the TPA effect, can therefore be expressed as follows [7–12]:

$$\Phi(t) = \ -\ 0.5(\alpha\, h\,(t) + \alpha_{CH} h_{CH}(t) + \alpha_{SHB} h_{SHB}(t) + \beta\alpha_{TPA} L S(t)) \tag{9}$$

The QF [7–17] and the related BER [19] are used to evaluate the performance of AO AND, XOR, NOR, OR, NAND, and XNOR logic operations employing CR-SOAs at 320 Gb/s. To achieve acceptable performance, the relevant BER must be kept below 10^{-9}, which requires a minimum value of QF = 6 [8–17]. The Adams' numerical approach implemented in Wolfram Mathematica® was employed to prepare and run all simulations.

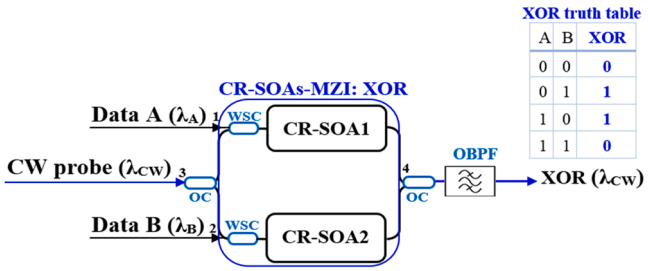


Fig. 1. XOR operation with CR-SOAs-MZI schematic diagram and truth table. OC: 3 dB optical coupler. WSC: wavelength selective coupler. CW: continuous wave. OBPF: optical bandpass filter.

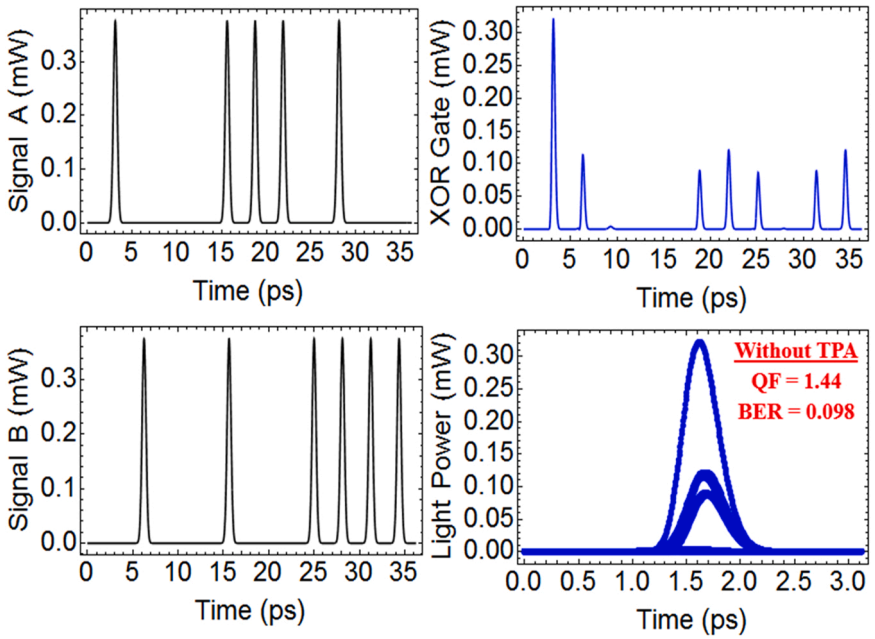


Fig. 2. Simulation results using CR-SOAs at 320 Gb/s for XOR logic gate without TPA.

3. Gates' implementation

3.1. XOR model

For XOR operation, data signals A and B, which serve as the pump, are launched into CR-SOA1 from port 1 and CR-SOA2 from port 2, respectively, via wavelength-selective couplers (WSCs). A 3 dB optical coupler (OC) splits a continuous wave (CW) beam acting as the probe into two components that enter CR-SOA1 and CR-SOA2, respectively, as shown in Fig. 1 [16]. The wavelength of the CW light (λ_{CW}) must be chosen so that it is different from the wavelength of signal A (λ_A) and the wavelength of signal B (λ_B). Cross-gain modulation (XGM) and cross-phase modulation (XPM) processes, which manifest in the CR-SOAs subject to the dynamical action of signals A and B, induce gain and phase changes on the CW beam components. When both A and B are '0′ or '1,' the CW output beams have the same gain and phase as they propagate across the two MZI arms, causing destructive interference at port 4 and resulting in '0′ at the output. When A is '0′ and B is '1′, or vice versa, the CW beams experience differing gain and phase modulations to constructively interfere at port 4, thereby resulting in'1′at the output. If only one of the inputs A or B is '1′, the optical circuit produces a '1′ at its output, as shown in the attached XOR truth table. This procedure is analogous to the XOR logic, the result of which is imprinted on the outgoing CW light at λ_{CW} determined by an optical bandpass filter (OBPF).

The input powers inside each CR-SOA for XOR gate are expressed as [16]:

$$P_{in,\ CR-SOA_1}(t) = P_A(t) + 0.5\,P_{CW} \tag{10}$$

$$P_{in,\ CR-\ SOA_2}(t) = P_B(t) + 0.5\,P_{CW} \tag{11}$$

where the coupling of the CW beam of power P_{CW} into the middle arm of the CR-SOAs-MZI is taken into consideration by the coefficient

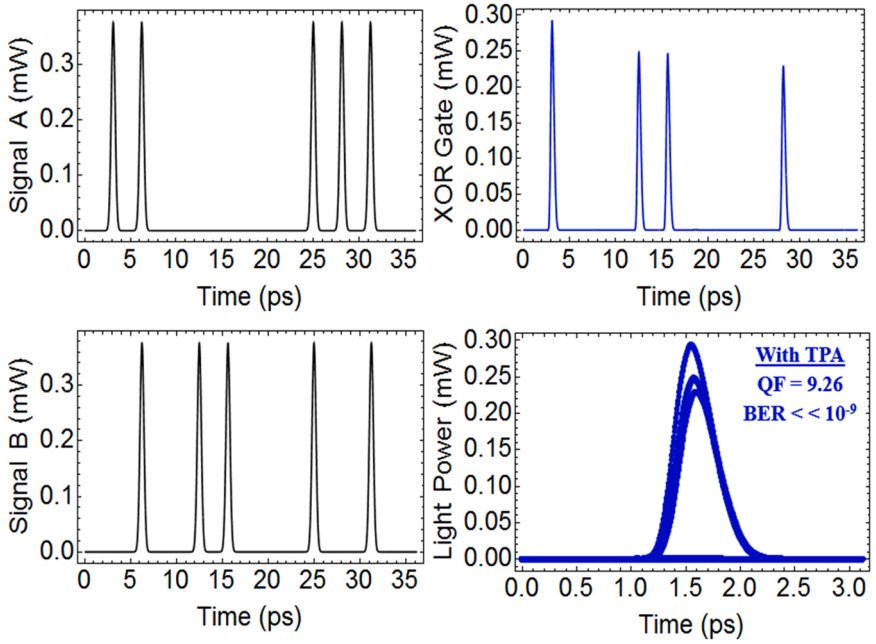


Fig. 3. Simulation results using CR-SOAs at 320 Gb/s for XOR logic gate with TPA.

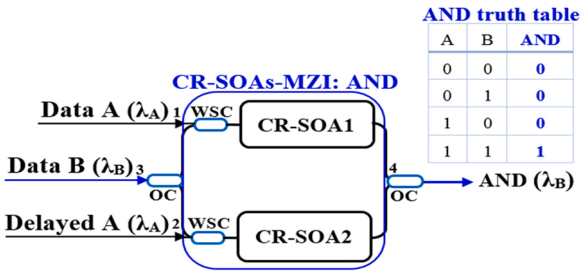


Fig. 4. AND operation using CR-SOAs-MZI schematic diagram and truth table.

'0.5'.

The modulated CW probe beams from the two arms of the CR-SOAs-MZI interfere according to the formula below [16]:

$$P_{XOR}(t) = 0.25\,P_{CW}\left(\begin{matrix} G_{CR-SOA_1}(t) + G_{CR-SOA_2}(t) - 2\sqrt{G_{CR-SOA_1}(t)\,G_{CR-SOA_2}(t)} \\ cos\left[\Phi_{CR-SOA_1}(t) - \Phi_{CR-SOA_2}(t)\right] \end{matrix}\right) \tag{12}$$

where $G_{CR\text{-}SOA1,2}(t)$ and $\Phi_{CR\text{-}SOA1,2}(t)$ are, respectively, the gains and phase responses of the CR-SOA1 and CR-SOA2.

The simulation results for the AO XOR operation employing CR-SOAs-MZI without TPA and with TPA at 320 Gb/s are shown in Figs. 2 and 3, respectively. These findings show that using TPA, it is possible to implement a specific Boolean operation with better QF and BER than it would be without it. Because the carrier recovery dynamics in the CR-SOAs are enhanced in the presence of TPA, the peak amplitude fluctuations are strongly suppressed, while the form of the corresponding pseudo-eye diagram is significantly improved.

3.2. AND model

Data A and its delayed copy are injected into each of the two CR-SOAs through WSCs to perform the AND operation (ports 1 and 2 in Fig. 4). Data B, which is spectrally located at a different wavelength, is fed into both CR-SOA1 and CR-SOA2 via a 3 dB OC (port 3 in Fig. 4) [15]. A phase window is created for data B using data A and its delayed version. This phase window is closed when A = '0' and B = '1' or '0,' hence the result should be '0'. However, when both A and B are '1' the phase window opens and forces the split counterparts of data B to interfere constructively, which results in a switched value of '1'. As a result, a logical '1' is acquired only when both A and B are '1,' which, according to the related truth table, is functionally equivalent to an AO AND logic operation.

The total input powers going into CR-SOA1 and CR-SOA2 to implement the AND gate are expressed as follows [15]:

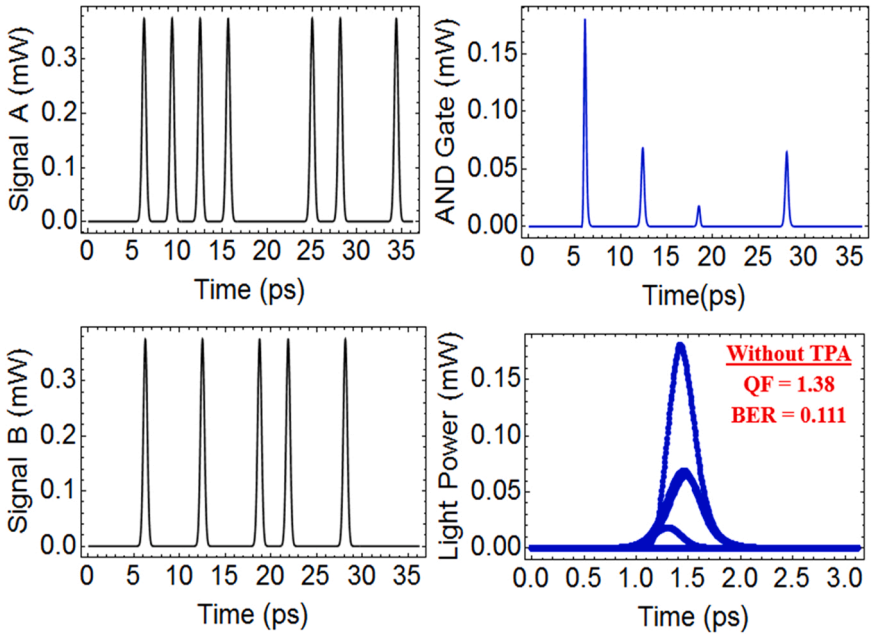


Fig. 5. Simulation results using CR-SOAs at 320 Gb/s for AND logic gate without TPA.

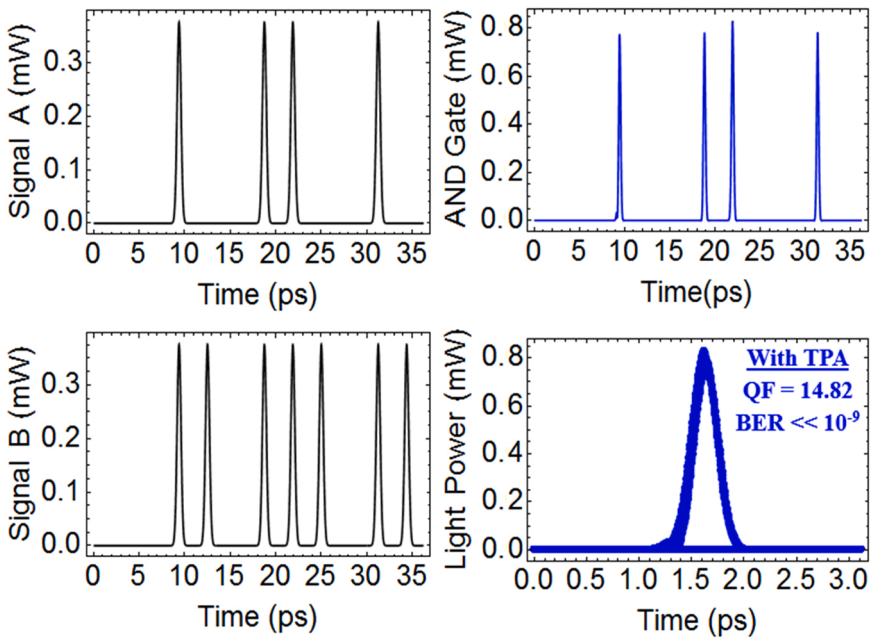


Fig. 6. Simulation results using CR-SOAs at 320 Gb/s for AND logic gate with TPA.

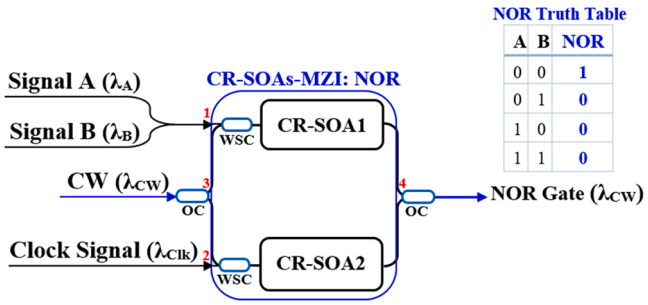


Fig. 7. NOR gate using CR-SOAs-MZI schematic diagram and truth table.

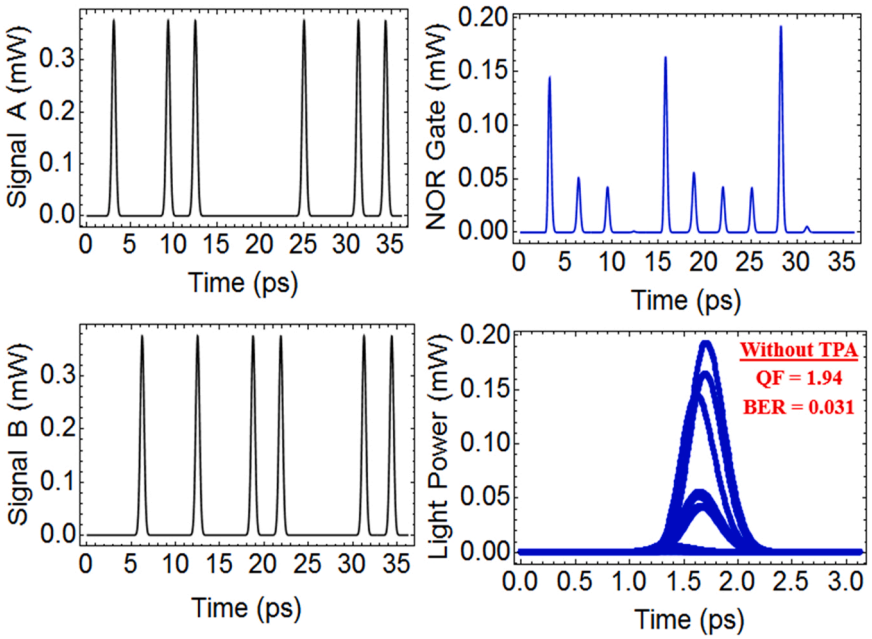


Fig. 8. Simulation results using CR-SOAs at 320 Gb/s for NOR logic gate without TPA.

$$P_{in,\ CR-SOA_1}(t) = P_A(t) + 0.5\,P_B(t) \tag{13}$$

$$P_{in,\ CR-SOA_2}(t) = P_A(t-\Delta\tau) + 0.5\,P_B(t) \tag{14}$$

where $\Delta\tau$ is the time delay for delayed signal A.

The interferometric equation that describes the AND output power is as follows [15]:

$$P_{AND}(t) = 0.25\,P_B(t)\left(G_{CR-SOA_1}(t) + G_{CR-SOA_2}(t) - 2\sqrt{G_{CR-SOA_1}(t)\,G_{CR-SOA_2}(t)}\ cos\left[\Phi_{CR-SOA_1}(t) - \Phi_{CR-SOA_2}(t)\right]\right) \tag{15}$$

Figs. 5 and 6 illustrate the simulation results of AND operation and its corresponding eye diagram utilizing CR-SOAs-based MZI at 320 Gb/s without TPA and with TPA, respectively. These results indicate that the scheme can only yield quantitatively and qualitatively superior and acceptable outcomes when TPA is present in CR-SOAs.

3.3. NOR model

In order to perform NOR, input data signals A and B are combined and injected into port 1 in Fig. 7(i.e. CR-SOA1) through WSC, while the Clk is injected into port 2 (i.e. CR-SOA2). Concurrently, a CW beam is divided by a 3 dB OC into two halves to enter distinctly CR-SOA1 and CR-SOA2 at port 3. Signals A and B modulate the CW gain and phase through XGM and XPM nonlinear effects. Thus, when a combination of high power signals (01, 10, or 11) is sent to CR-SOA1 and a Clk (all 1's) is sent to CR-SOA2, both CR-SOAs become saturated. Therefore, the modulated phase of the CW components encounters identical dynamic properties, so that they

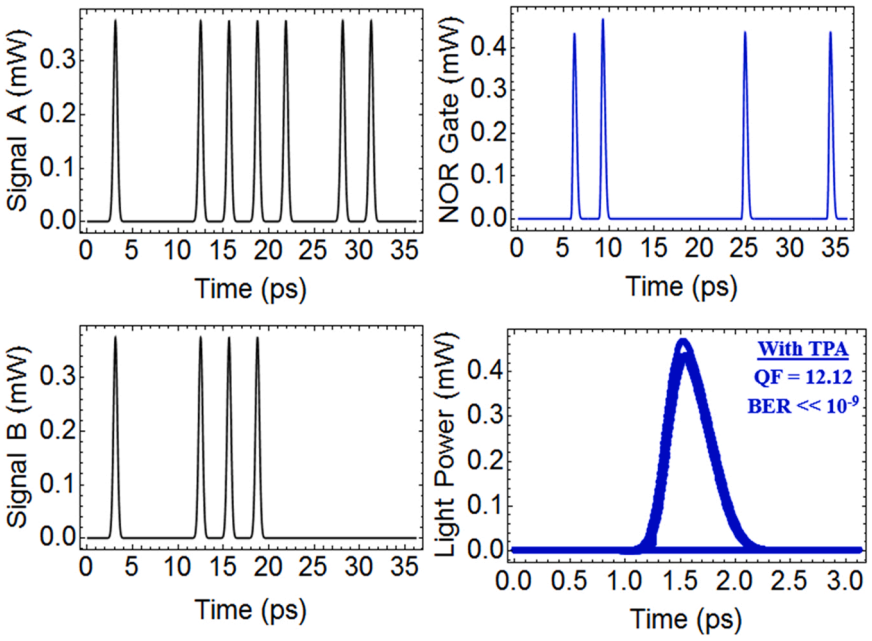


Fig. 9. Simulation results using CR-SOAs at 320 Gb/s for NOR logic gate with TPA.

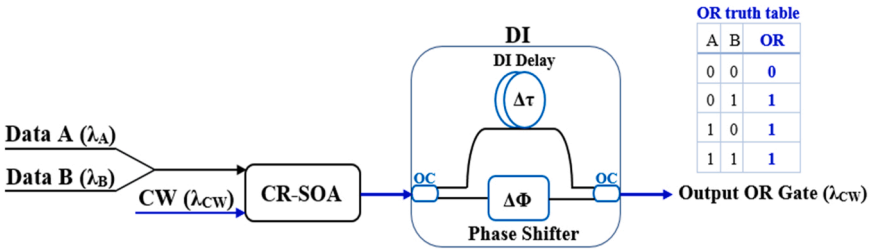


Fig. 10. OR gate using CR-SOA-DI schematic diagram and truth table.

interfere destructively at the output, thus resulting in a logical '0'. The Clk will break the phase balance of the CR-SOAs-MZI if low power signals' combination (00) is launched, resulting in a logical '1' appearing at port 4 owing to constructive interference. As a result, the Boolean NOR logic gate is realized according to its truth table.

The optical powers entering CR-SOA1 and CR-SOA2 are, respectively, expressed as follows [18]:

$$P_{in,\ CR-SOA_1}(t) = P_A(t) + P_B(t) + 0.5\,P_{CW} \tag{16}$$

$$P_{in,\ CR-SOA_2}(t) = P_{Clk}(t) + 0.5\,P_{CW} \tag{17}$$

Then, the NOR output power is given by [18]:

$$P_{NOR}(t) = 0.25\,P_{CW}\left(\begin{matrix} G_{CR-SOA_1}(t) + G_{CR-SOA_2}(t) - 2\sqrt{G_{CR-SOA_1}(t)\ G_{CR-SOA_2}(t)} \\ cos\left[\Phi_{CR-SOA_1}(t) - \Phi_{CR-SOA_2}(t)\right] \end{matrix}\right) \tag{18}$$

Figs. 8 and 9 show the simulation results and related eye diagram for NOR operation using CR-SOAs-MZI at 320 Gb/s without and with TPA, respectively.

3.4. OR model

As shown in Fig. 10 [14], data signals A, B, and a CW beam are merged and supplied into the CR-SOA followed by a DI, for OR operation. Signals A and B in the CR-SOA use XPM to induce the phase of the CW signal. After exiting the CR-SOA, the CW signal is split into two halves by a 3 dB OC before entering a DI, where the delay time ($\Delta\tau_{DI}$) and phase bias ($\Delta\Phi_{DI}$) are adjusted to induce a phase difference between the CW constituents. When A = B = '1' and A = '0', B = '1', or vice versa, the CW components are arranged to lie within the created phase window and are forwarded at the DI output, producing logical '1's. The CW components that have not

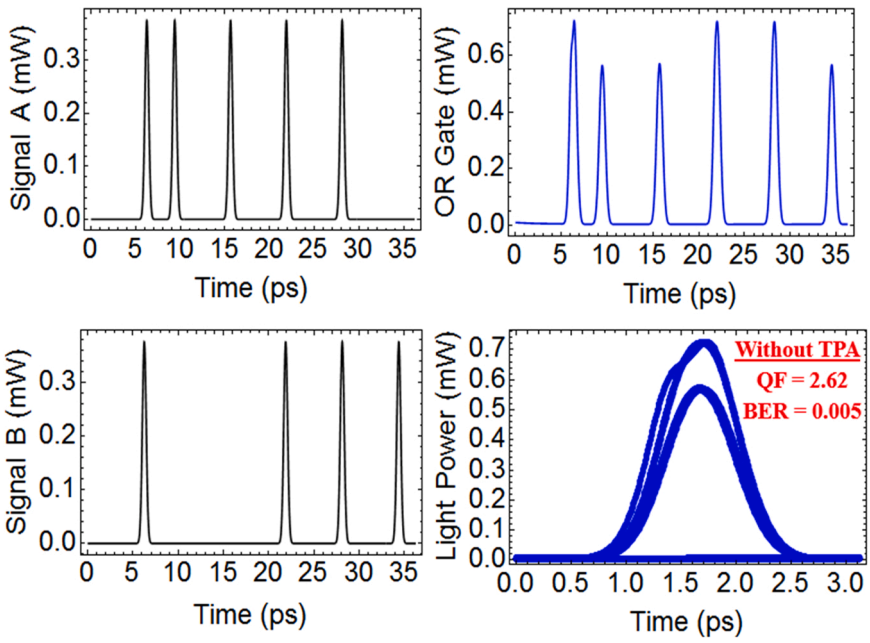


Fig. 11. Simulation results using CR-SOA at 320 Gb/s for OR logic gate without TPA.

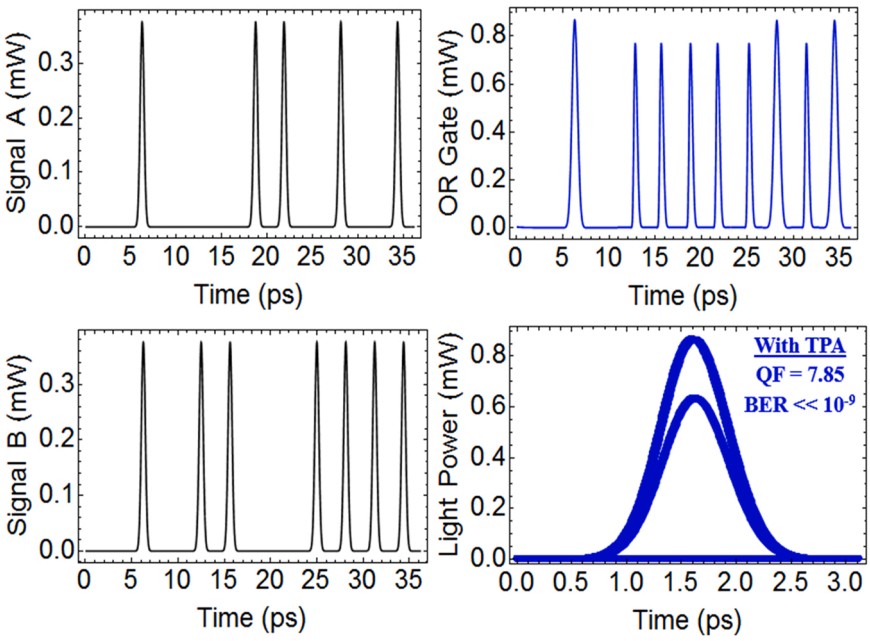


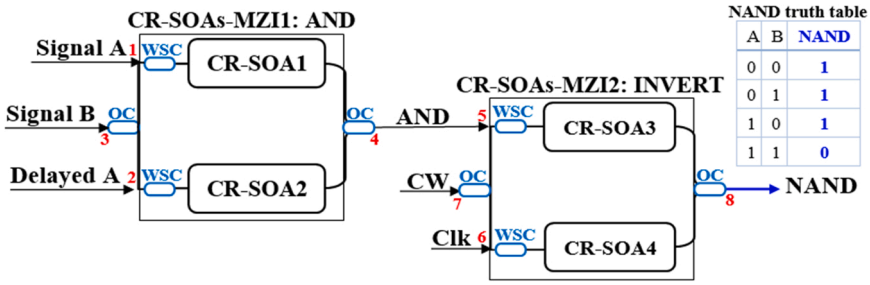
Fig. 12. Simulation results using CR-SOA at 320 Gb/s for OR logic gate with TPA.

undergone a phase shift, on the other hand, are pushed outside the phase window, suppressed at the DI output, and result in '0's. As a result, the OR truth table is achieved, which is the desired outcome.

Because the input signals A, B, and the CW beam are all connected to the CR-SOA, the total input power is stated as [14]:

$$P_{in,\,CR-SOA}(t) = P_A(t) + P_A(t) + P_{CW} \tag{19}$$

The following basic interferometric formula defines the DI's output power for OR operation [14]:



NAND truth table

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 13. NAND gate using CR-SOAs-MZIs schematic diagram and truth table. Clk: clock signal (all '1's).

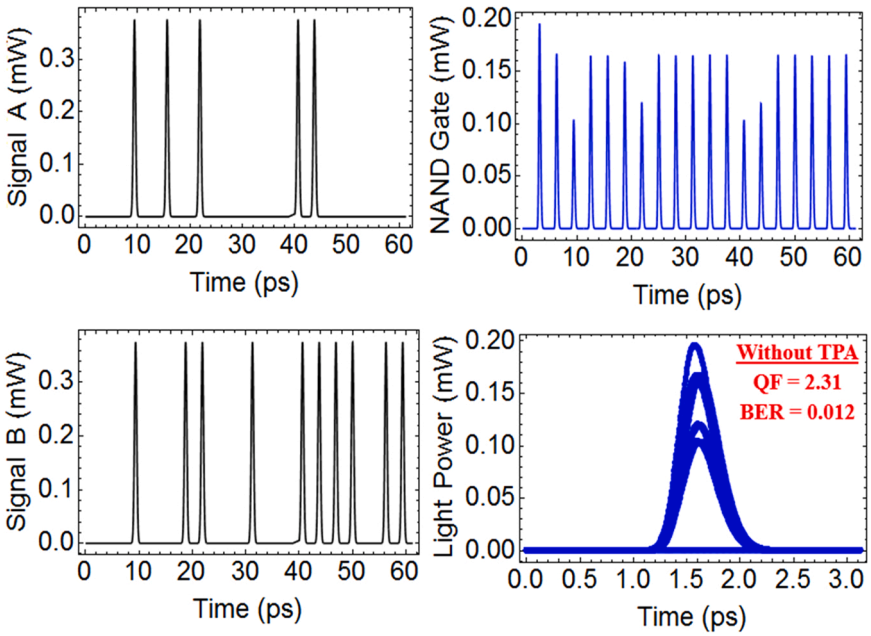


Fig. 14. Simulation results using CR-SOAs at 320 Gb/s for NAND logic gate without TPA.

$$P_{OR}(t) = 0.25 \left(\begin{array}{l} P_{out,\ CR-SOA}(t) + P_{out,\ CR-SOA}\left(t - \Delta\tau_{DI}\right) - 2\sqrt{P_{out,\ CR-SOA}(t)\, P_{out,\ CR-SOA}\left(t - \Delta\tau_{DI}\right)} \\ cos\left[\Phi_{out,\ CR-SOA}(t) - \Phi_{out,\ CR-SOA}\left(t - \Delta\tau_{DI}\right) + \Delta\Phi_{DI}\right] \end{array} \right) \quad (20)$$

where $\Delta\tau_{DI}$ and $\Delta\Phi_{DI}$ are the DI delay time and phase bias.

Figs. 11 and 12 demonstrate the pulse patterns of data input A and B, the OR logic gate output, and the OR eye diagram at 320 Gb/s using CR-SOA-DI without and with TPA, respectively. These outcomes show that TPA can be used to achieve acceptable QF and BER for this Boolean operation, while this is not possible without TPA.

3.5. NAND model

As shown in Fig. 13 [17], the NAND operation is achieved through a sequence of AND and INVERT operations, which are implemented by the CR-SOAs-MZI1 and CR-SOAs-MZI2, respectively. The AND output, which was previously discussed in Section 4, is directed into CR-SOAs-MZI2 to undergo the INVERT operation. When one of the data inputs is replaced by a Clk signal, the INVERT operation is equivalent to the XOR operation. The result of A NAND B logic is thus acquired from the CR-SOAs-MZI2 output.

The input signal powers into CR-SOA3 and CR-SOA4 are expressed as follows for INVERT operation [17]:

$$P_{in,\ CR-SOA_3}(t) = P_{AND}(t) + 0.5P_{CW} \quad (21)$$

$$P_{in,\ CR-SOA_4}(t) = P_{Clk}(t) + 0.5P_{CW} \quad (22)$$

Then, at the CR-SOAs-MZI2 output, the power of the NAND operation is described by [17]:

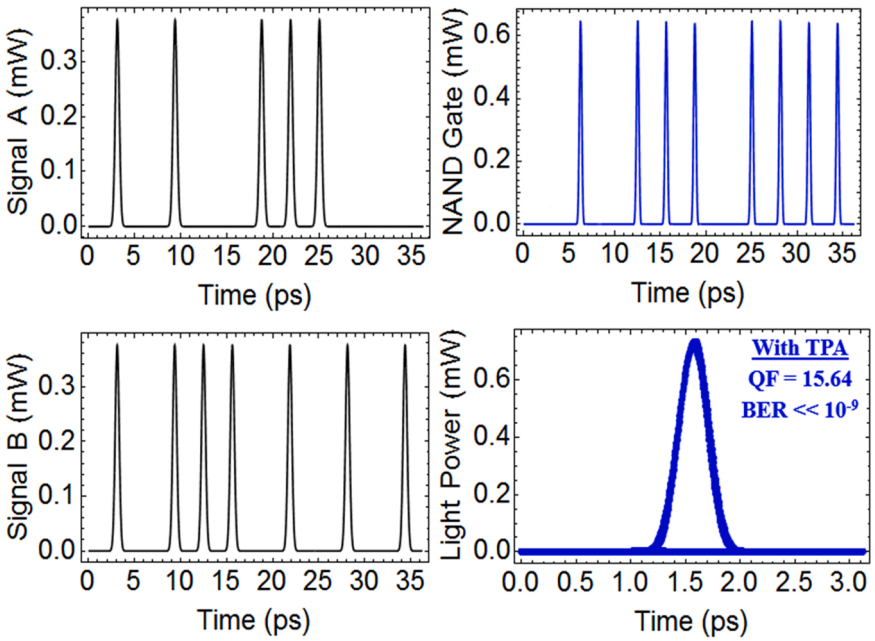


Fig. 15. Simulation results using CR-SOAs at 320 Gb/s for NAND logic gate with TPA.

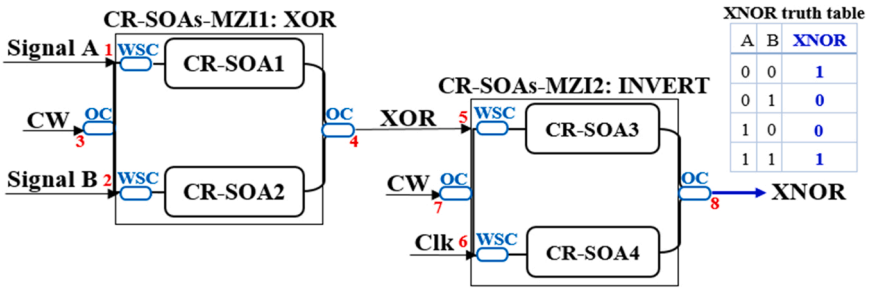


Fig. 16. XNOR gate using CR-SOAs-MZIs schematic diagram and truth table.

$$P_{NAND}(t) = 0.25\,P_{CW}\left(\begin{matrix} G_{CR-SOA_3}(t) + G_{CR-SOA_4}(t) - 2\sqrt{G_{CR-SOA_3}(t)\;G_{CR-SOA_4}(t)} \\ cos\left[\Phi_{CR-SOA_3}(t) - \Phi_{CR-SOA_4}(t)\right] \end{matrix}\right) \tag{23}$$

Figs. 14 and 15 demonstrate the simulation results for the NAND operation employing CR-SOAs-MZIs at 320 Gb/s without and with TPA, respectively. Without the TPA effect, the eye diagram is strongly deformed; With TPA, however, the eye diagram is restored to resemble that of the input data signals.

3.6. XNOR model

As shown in Fig. 16 [17], the XNOR logic gate is implemented via a sequence of XOR and INVERT operations carried out by two cascaded CR-SOAs-MZIs. The XOR gate output and a Clk signal are launched into CR-SOA3 and CR-SOA4, respectively, to perform the INVERT operation, while a CW beam is injected into the middle of CR-SOAs-MZI2. Consequently, the A XNOR B logic gate outcome is obtained from OC at port 8.

For the INVERT operation required to achieve the XNOR function, the input powers inside CR-SOA3 and CR-SOA4 are stated as follows [17]:

$$P_{in,\,CR-SOA_3}(t) = P_{XOR}(t) + 0.5\,P_{CW} \tag{24}$$

$$P_{in,\,CR-SOA_4}(t) = P_{Clk}(t) + 0.5\,P_{CW} \tag{25}$$

The XNOR power output from CR-SOAs-MZI2 is then defined as follows [17]:

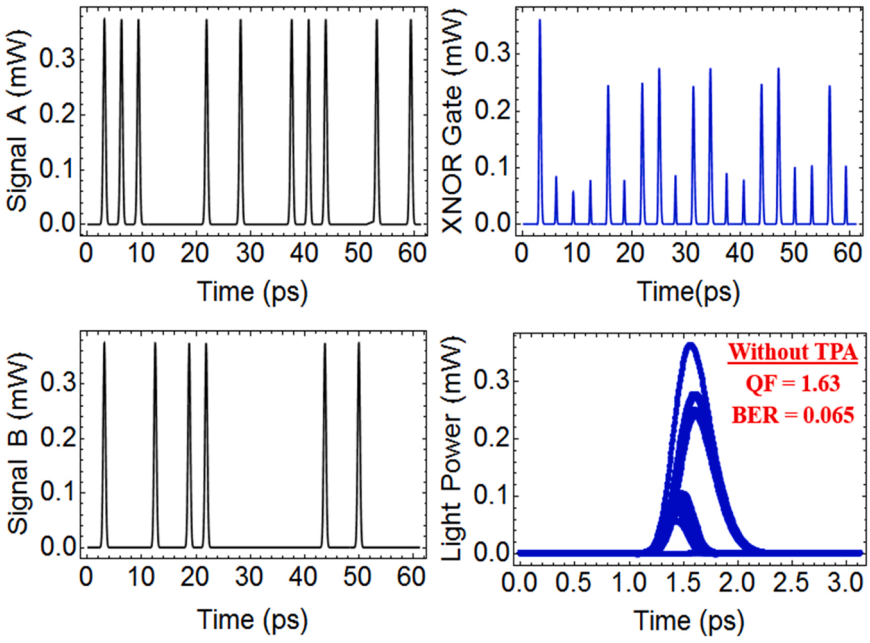


Fig. 17. Simulation results using CR-SOAs at 320 Gb/s for XNOR logic gate without TPA.

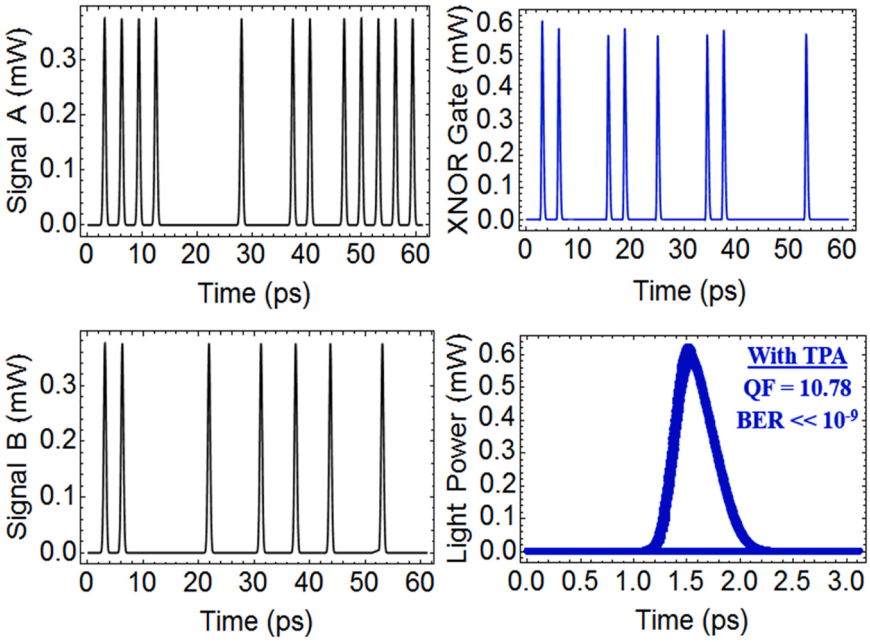


Fig. 18. Simulation results using CR-SOAs at 320 Gb/s for XNOR logic gate with TPA.

$$P_{XNOR}(t) = 0.25\,P_{CW}\left(\begin{matrix} G_{CR-SOA_3}(t) + G_{CR-SOA_4}(t) - 2\sqrt{G_{CR-SOA_3}(t)\;G_{CR-SOA_4}(t)} \\ cos\left[\Phi_{CR-SOA_3}(t) - \Phi_{CR-SOA_4}(t)\right] \end{matrix}\right) \tag{26}$$

Figs. 17 and 18 depict the numerical results for the AO XNOR logic gate with and without TPA, respectively, when employing CR-SOAs-MZIs at 320 Gb/s. The TPA still proves that it should be exploited to enable logic operation with improved performance at ultra-high speeds.

The ASE noise affects the (CR)-SOA dynamics by consuming carriers for self-amplification, a phenomenon that is governed by the propagating pulses' properties and is dependent on the carriers' spatial and temporal distribution. Therefore, the ASE influence on the

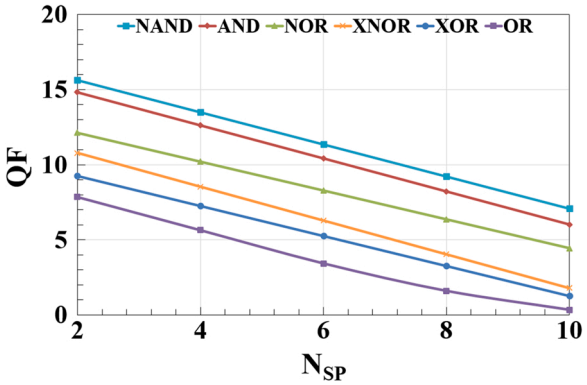


Fig. 19. QF versus spontaneous emission factor (N_{SP}) for AO considered operations using CR-SOAs at 320 Gb/s with TPA.

Table 2
Comparison of theoretically implemented AO logic gates using various (CR)-SOAs-based schemes and data rates.

Operation	Scheme	Data rate (Gb/s)	QF	Ref.
XOR	SOAs	80	8.7	[20]
	SOAs-TPA	250	9.8	[9]
	CR-SOAs	100	18.5	[16]
	CR-SOAs	320	1.44	This work
	CR-SOAs-TPA	320	9.26	This work
AND	SOAs	80	7	[21]
	SOAs-TPA	250	10.8	[12]
	CR-SOAs	100	14	[15]
	CR-SOAs	320	1.38	This work
	CR-SOAs-TPA	320	14.82	This work
NOR	SOAs	80	8.2	[20]
	SOAs-TPA	250	14	[10]
	CR-SOAs	100	15.6	This work
	CR-SOAs	320	1.94	This work
	CR-SOAs-TPA	320	12.12	This work
OR	SOA	80	7	[20]
	SOA-TPA	250	9	[11]
	CR-SOA	100	9	[14]
	CR-SOA	320	2.62	This work
	CR-SOA-TPA	320	7.85	This work
NAND	SOAs	80	7	[20]
	SOAs-TPA	250	8.2	[12]
	CR-SOAs	120	13.5	[17]
	CR-SOAs	320	2.31	This work
	CR-SOAs-TPA	320	15.64	This work
XNOR	SOAs	80	10.2	[22]
	SOAs-TPA	250	12.34	[12]
	CR-SOAs	120	12.4	[17]
	CR-SOAs	320	1.63	This work
	CR-SOAs-TPA	320	10.78	This work

operations' performance should be calculated as done in Fig. 19, which depicts the QF versus the spontaneous emission factor (N_{SP}) in the presence of TPA nonlinear effect. The ASE [18] noise is added numerically to the gates' output powers to obtain the QF. It can be demonstrated that the QF decreases significantly as the N_{SP} increases, but we note that the CR-SOA resists this effect and still gives an acceptable performance even at higher values of N_{SP}. This happens because the TPA enhances the CR-SOAs dynamics, resulting in improving the gates' QF.

Table 2 summarizes the various schemes and data rates reported in the literature for theoretically implemented AO XOR, AND, NOR, OR, NAND, and XNOR logic operations employing (CR)-SOAs. The AND, XOR, NOR, NAND, and XNOR have been implemented with (CR)-SOAs-based MZIs, while the OR operation with (CR)-SOA-based DI. All the works included in the comparison have used (CR)-SOAs and associated nonlinear effects to design the target AO gates. This ensures a fair and consistent comparison. When TPA is accounted for as a nonlinear effect in traditional SOAs and CR-SOAs modeling, the higher QF values are produced. The TPA can also be used to increase the speed of certain logic functions.

The experimental verification of the proposed logic structures using CR-SOAs could be done according to the main outcomes of our study, given that the relevant technology is available. This would require to control (1) the level of the input data peak power, and (2) the degree of the phase difference between the arms of MZI, so that in both cases conditions favorable for switching can be created. This

is not a fundamental barrier, but rather a technological issue that may be addressed in practice. Issue (1) can be addressed with commercially available erbium-doped fiber amplifiers. On the other hand, for issue (2), the differential phase should be fine-tuned to fall within the required interval based on the binary combination of the input data and the logic output expected from each target gate's truth table [23]. This can be accomplished by using active phase shifters after each CR-SOA to provide an additional phase difference between the upper and lower MZI arms [24] for optimal switching. These shifters are thermo-optic elements with low tuning voltage and power dissipation [25] and can be incorporated into the same planar lightwave circuit substrate with CR-SOAs-based devices [26]. These guidelines concern the considered AO gates except for the OR, for which the required DI is also technologically available [27].

4. Conclusion

This work investigates and evaluates the performance of Boolean XOR, AND, NOR, OR, NAND, and XNOR logic functions in CR-SOAs at 320 Gb/s, taking into account the TPA nonlinear effect. To perform the XOR, AND, NOR, NAND, and XNOR operations, CR-SOAs are incorporated in configured MZIs, which are assisted by a DI for OR operation. The simulation results show that these logic gates can be implemented at 320 Gb/s with far better QF and BER when TPA is considered in CR-SOAs, while without TPA this is not possible since the metrics are seriously degraded.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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