ADVANCED FUNCTIONAL MATERIALS
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Multifunctional $MoTe_2$ Fe-FET Enabled by Ferroelectric Polarization-Assisted Charge Trapping

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The "Internet-of-Things"-based information society requires the devices to possess high scaling capability as well as rich functionalities. Hybrid systems coupling 2D semiconductors and functional ferroelectrics are attracting increasing attention as complementary devices to the existing silicon systems due to their outstanding electronic and optoelectronic performances. In this work, interfacial states are introduced on the ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ thin film during the annealing process. Utilizing the synergetic effect of ferroelectric polarization and charge trapping behavior, a multifunctional 2D Fe-FET is demonstrated, exhibiting reliable memory properties, tunable synaptic functions, and reconfigurable photodetection behaviors in one single device. Among them, multiple storage levels are achieved with a long retention time. Flexible plasticity including short-term plasticity (STP)/long-term plasticity (LTP) is emulated successfully, and the excellent emulated synaptic behaviors also contribute to the pattern recognition accuracy of ≈81% in artificial neural network simulations. Furthermore, the ferroelectric polarization-dependent optoelectronic response is observed, making it promising for the optoelectronic logic device application. The results pave the way for the fabrication of high-density data process systems with various functions.

1. Introduction

With the rapid evolution of microelectronic technology and the increasing demand for functional devices for data-centric applications, shrinking the characteristic size or increasing the functionalities of one single device is greatly desired,[1–5] particularly for central process units, memory, and image sensors as well as neuromorphic devices. Recently, considerable interest has been dedicated to hybrid electronic devices coupling two-dimensional (2D) materials, e.g., graphene, with different ferroelectric materials, like poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)],[6–7] lead zirconium titanate ($Pb(Zr,Ti)O_3$, PZT) and other complex oxides with perovskite structure for memory and logic applications.[8–9] Atomically thin 2D semiconductors possessing diverse electronic, optoelectronic, and mechanical properties can be suitable beyond-silicon options for the semiconductor industry.[10–11] In addition, the difficulty in achieving ferroelectric/silicon interfaces with high structural quality when integrating the ferroelectric field-effect transistor (Fe-FET) devices into CMOS technology can be potentially addressed because of the strong covalent bonds within 2D materials, making chemically stable interface possible. More importantly, the large surface-to-volume ratio of 2D semiconductors makes them highly sensitive to their surface and interface environment,

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The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adfm.202110415.

DOI: 10.1002/adfm.202110415

which greatly enhances their response to external stimuli.[12–13] In the hybrid 2D materials/ferroelectrics systems, the interplay between the intrinsic ferroelectric polarization switching in the ferroelectric materials and charge dynamics behaviors at the interface states may be leveraged to introduce novel electrical and optoelectrical features.

Ferroelectric materials have become an important part of advanced microelectronics since their successful integration with the semiconductor industry.[14–15] However, widespread application of the thin film ferroelectric materials still faces serious challenges because of the reduced long-range Coulomb coupling and the strengthened depolarization electrostatic field when the thickness of the film drops to several or tens of nanometer.[16–17] Recently, the discovery of ferroelectricity in doped HfO_2 ushered in a pathway for ferroelectric-based electronic devices in high volume semiconductor manufacturing by providing a possible solution to bridge the scaling gap between perovskite ferroelectric materials and Si-based semiconductor technology.[14,18]

Therefore, hybrid systems based on 2D semiconductors and HfO_2-based ferroelectric thin film provide the possibilities for the development of next-generation functional devices with ultrathin dimensionality, enhanced performance, and rich functionalities. Particularly in transistor-like device configuration, carriers in the 2D materials channel can be modulated by the ferroelectric polarization of the adjacent ferroelectrics,[19] showing appealing characteristics for its application in non-volatile memory and logic devices with low-power consumption.

Here, we report a multifunctional 2D Fe-FET device employing 2D $MoTe_2$ and ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin film. The effects of interfacial charges on the electronic transport and optoelectrical response in the $MoTe_2$-HZO Fe-FET are demonstrated. Clockwise hysteresis behavior attributed to the charge trapping on annealing-introduced surface states in HZO is observed in transfer characteristics, which can be evidenced by the ultraviolet photoelectron spectroscopy (UPS) measurement. The reliable non-volatile memory performance can be achieved due to the synergetic effect of ferroelectric polarization and charge trapping behavior. Moreover, the device can also function as an artificial synapse showing flexibly modulated plasticity behaviors, such as short-term plasticity (STP) and long-term plasticity (LTP) characteristics. A fully connected neural network (FNN) model is also simulated to conduct recognition of the handwritten digital pattern, showing an accuracy of 81%. Furthermore, the device demonstrates unique optoelectronic properties, which shows the ferroelectric polarization-dependent optoelectrical response feature, making it promising for optoelectronic logic device applications. Considering the complementary metal-oxide-semiconductor (CMOS) technology compatibility of HZO and the possibility for the large-scale growth and transfer of 2D materials,[20–21] our results shed light on the fabrication of high-density data process systems with various functions.

2. Results and Discussion

2.1. Device Working Mechanism and Electrical Characterizations

The 2D Fe-FET device was constructed by utilizing a 20 nm HZO as the gate dielectric and dry transferring a two-dimensional $MoTe_2$ flake onto it. The used 20-nm-thick HZO thin film was grown on the Si substrate by the atomic layer deposition method followed by annealing in an N_2 atmosphere at 400 °C for 2 h. The schematic diagram and optical image of the 2D Fe-FET device can be found in **Figure 1**a and Figure S1a in the Supporting Information, respectively. Atomic force microscopy (AFM) image of the device displayed in Figure S1b in the Supporting Information determines the channel thickness to be around 10.6 nm, corresponding to ≈11 layers.

The ferroelectric and insulating characteristics of the HZO film were verified first. Piezoresponse force microscopy (PFM) measurement was conducted to characterize its ferroelectricity properties. Figure S2a,b in the Supporting Information display the out-of-plane (OOP) PFM amplitude and phase images under the DC written bias (tip bias: ± 9 V). The obvious phase reversal can be observed after applying the opposite voltage force, verifying the existence of the switchable ferroelectric polarization in HZO film. The local ferroelectric polarization switching of HZO in the OOP direction is displayed in Figure 1b. The PFM phase (black dots) loop with the 180° phase-contrast together with the prominent amplitude (red dots) hysteresis loop further confirm the switchable ferroelectric polarization in the HZO film under an external electric field. Furthermore, the breakdown voltage of a 15 nm HZO was investigated based on the metal-insulator-metal (MIM) structure (Figure S2c, Supporting Information) to evaluate its feasibility as the dielectric for electronic devices. Figure S2d in the Supporting Information displays the measured I_{sd}–V_{sd} curve, where the I_{sd} first increases exponentially with V_{sd} and then rises abruptly to reach the compliance level (10^{-5} A) set by the source measurement unit at V_{sd} = 5.9 V. This voltage value is corresponding to a breakdown field of 4.0 MV cm^{-1}, which is comparable to the values in other commonly used dielectrics, confirming its capability to work as the dielectric.[22]

The electrical characterizations of the $MoTe_2$ Fe-FET were conducted. Figure 1c and Figure S3a in the Supporting Information display the transfer characteristics (I_{sd}–V_g) of the device by applying different V_g sweeping ranges and V_{sd} values, respectively, where the $MoTe_2$ Fe-FET shows obvious electron-dominated clockwise hysteresis behavior under forward and backward gate voltage (V_g) sweeping. It is worth mentioning that the results of conductance tuning in our 2D semiconductor channel by ferroelectric polarization are different from the behaviors in previous reports, which mostly show the anti-clockwise hysteresis for the n-type channel.[23–25] Clockwise hysteresis observed in previous studies were almost attributed to the adsorption of molecules,[26–27] oxide traps close to the 2D channel,[28–29] intrinsic traps,[30] and etc. As a result, we propose that the interface traps between the 2D $MoTe_2$ channel and HZO substrate are the possible origin for the observed clockwise hysteresis.

Schematic illustration of the hysteresis originated from a) pure ferroelectric polarization (P_r) switching and b) ferroelectric polarization assisted interfacial trapping effect are shown in Figure 1d (ii) and (iii), respectively. The corresponding transfer characteristics are displayed in Figure 1d (i) and (iv). Although the ferroelectric polarization in HZO is switched along the direction of the applied electric

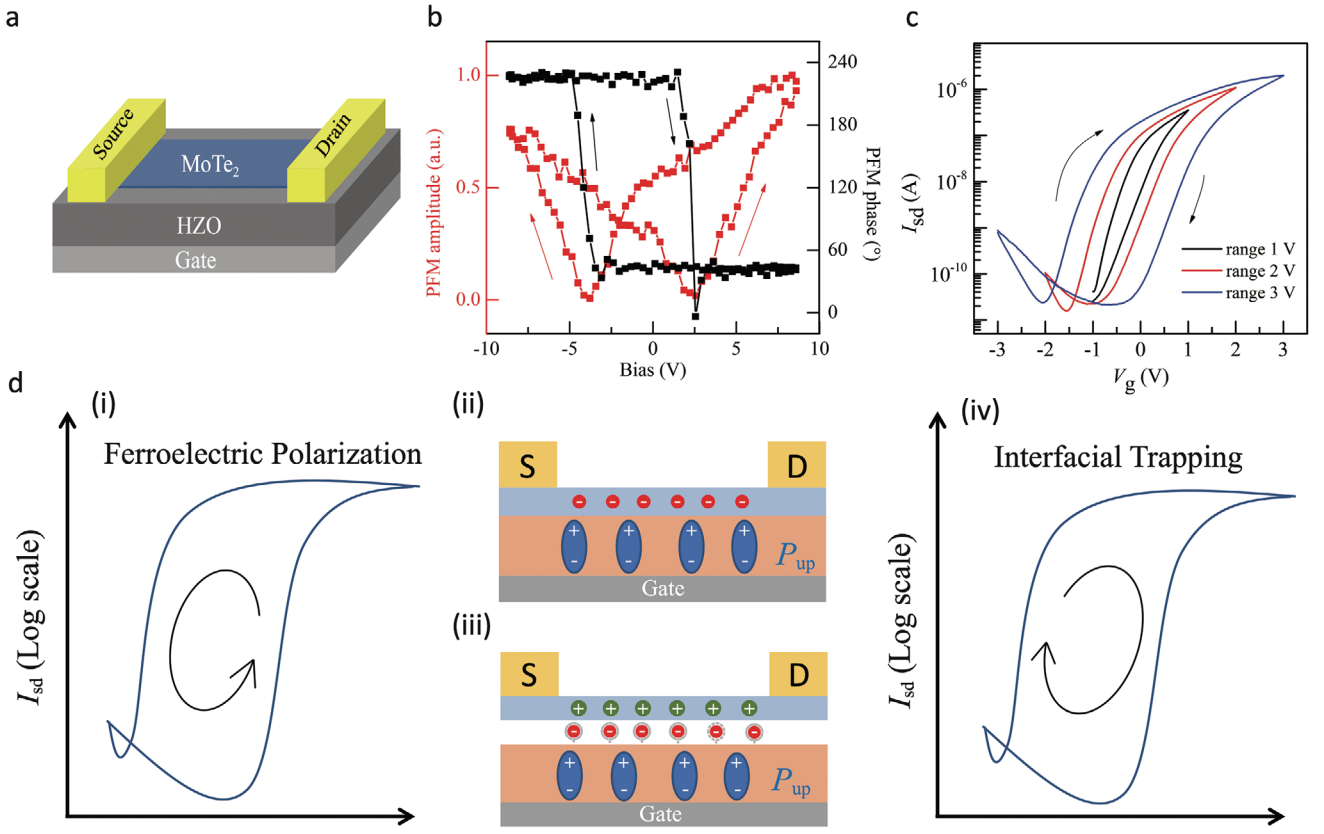

Figure 1. a) Schematic diagram of the 2D $MoTe_2$ Fe-FET device. b) Single point hysteresis loop obtained by SS-PFM method, the red line represents amplitude change and the black line represents phase change. c) Transfer characteristics (I_{sd}–V_g) of the device under different V_g sweeping ranges (±1 to ±3 V) at a fixed V_{sd} = 100 mV. The directions of the hysteresis loops are indicated by the arrows. d) Schematic image of the hysteresis originated from different mechanisms, in which (i), (ii) illustrate the anti-clockwise hysteresis rising from the switch of the ferroelectric polarization, and (iii), (iv) illustrate the clockwise hysteresis induced from ferroelectric polarization assisted interfacial trapping effect.

field, clockwise hysteresis appears because of the dominant carrier trapping behavior at the interface traps, which determines the transfer characteristics of the $MoTe_2$ Fe-FET. As shown in (iii) of Figure 1d, the initial positive bias in the backward sweeping process can attract electrons into these trap states from the $MoTe_2$ channel, thus leading to the electron depletion behavior in $MoTe_2$. Therefore, the $MoTe_2$ channel exhibits the off state when V_g sweeps to the 0 V. In contrast, for the forward sweeping from a large negative bias, trapped electrons are released from trap states and some holes are trapped at interface traps. As a result, electrons are accumulated in the $MoTe_2$ channel, turning the channel to on state at V_g = 0 V. Due to such P_r assisted interfacial trapping mechanism, clockwise hysteresis in the transfer characteristics can be observed. The corresponding anti-clockwise hysteresis controlled purely by the ferroelectric polarization switching in HZO (Figure 1d (ii)) is displayed in Figure 1d(i). Ferroelectric polarization in the HZO can be pointed to the downward direction (P_{down}) under the negative gate voltage, which depletes the electrons in the $MoTe_2$ channel and induces the positive shift of the threshold voltage (V_{th}). On the contrary, the upward polarization induces electrons in the $MoTe_2$ channel electrostatically, leading to the negative shift of the V_{th}. Therefore, the pure polarization switching results in anti-clockwise hysteresis.

For our device, the transfer characteristics measured at different V_g sweeping rates and temperatures (measured at other devices with the same configuration) also support the P_r assisted interfacial trapping mechanism. As shown in **Figure 2**a, the hysteresis window gradually increases with decreasing the sweeping rate, which is related to the carriers' trapping kinetics. In addition, the hysteresis behavior becomes more obvious with increasing the measurement temperature (Figure 2b), because charge carriers become more active under higher temperatures. The memory window defined as the difference of the threshold voltage (ΔV_{th}) can also be extracted from Figure 2b, which increases linearly with the temperature as displayed in Figure 2c. The clockwise hysteresis and the increased memory window at higher temperatures indicate that the appearance of the hysteresis is mainly due to interfacial trap states, which are probably arising from surface defect states on HZO induced by the annealing process. It is further confirmed by the UPS spectra of the pristine HZO film and the HZO film treated by 400 °C, as are shown in Figure 2d. In the valence band spectra, it can be observed that the signals near the Fermi level appear after annealing treatment, indicating the generation of the surface states. Moreover, as indicated in Figure S4 in the Supporting Information, the density of surface states can be changed by the annealing conditions such as temperature and

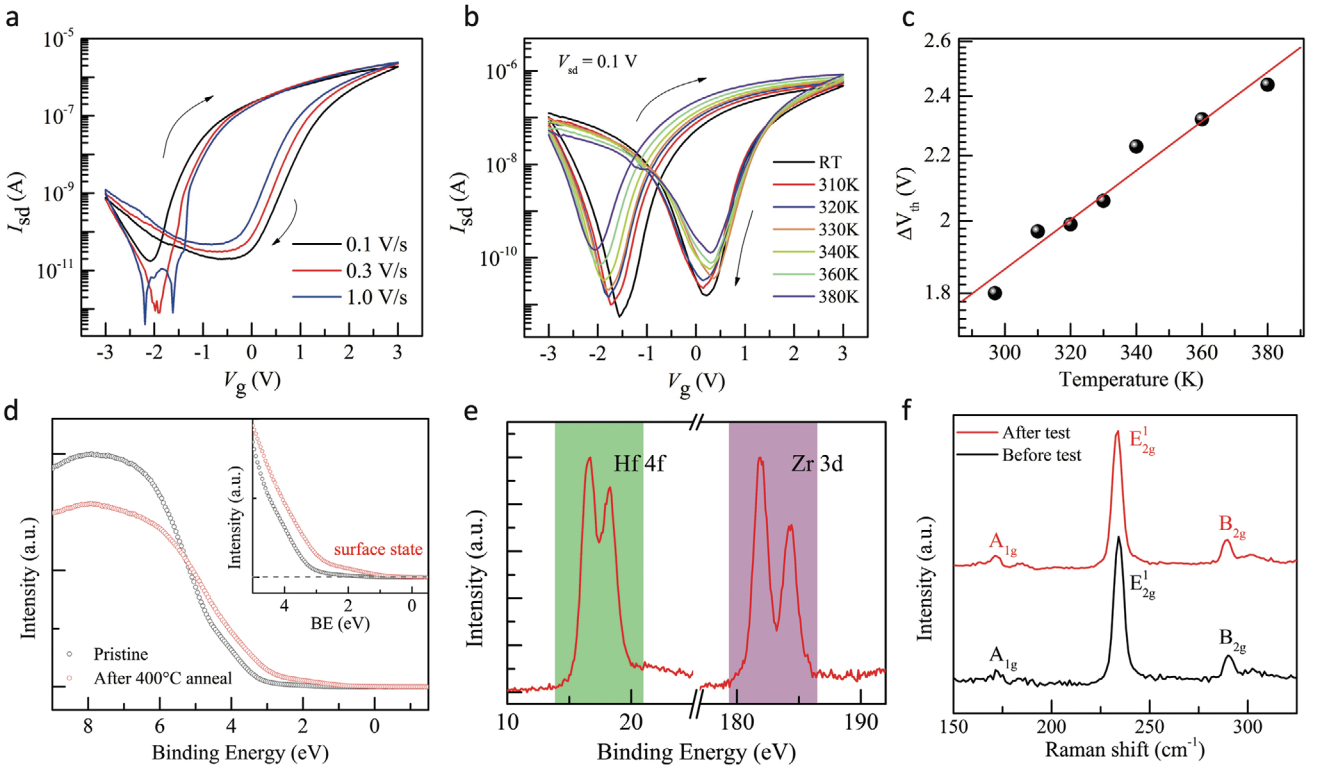

Figure 2. a) I_{sd}–V_g curves of the device under different V_g sweeping rates. b) I_{sd}–V_g curves of the device measured at different temperatures. c) Extracted memory window (difference in the threshold voltage) as a function of measurement temperature. d) UPS spectra for the valence band of the pristine and after 400 °C annealed HZO film. e) XPS spectra for the core levels of Hf 4f and Zr 3d. f) Raman spectra of the channel material (2H-$MoTe_2$) before and after the test, in which the characteristic peaks remain the same.

duration. Utilizing the electrical transfer curves of the devices (Figure S5, Supporting Information), the density of trap states is estimated to be around 1.30×10^{12}–1.37×10^{12} eV^{-1} cm^{-2}.[31] The Hf/Zr ratio can be determined from the X-ray photoelectron spectroscopy (XPS) spectrum (Figure 2e) with the value of about 1.02, indicating the $Hf_{0.5}Zr_{0.5}O_2$ composition of the sample. It is worth mentioning that the phase transition of the 2H-$MoTe_2$ is excluded. Before the test, the Raman spectra of the $MoTe_2$ flake (black curve, Figure 2f) shows three characteristic peaks at 171.2 cm^{-1} (A_{1g}), 233.9 cm^{-1} (E_{2g}^1), and 289.6 cm^{-1} (B_{2g}), indicating its 2H crystal phase.[32] After performing all the electrical and optoelectrical measurements, the Raman spectra does not show obvious variations (red line, Figure 2f). Therefore, the clockwise hysteresis of our results is attributed to the ferroelectric polarization-assisted interfacial trapping effect of HZO.

The control devices have been investigated to confirm the proposed working mechanism (Figure S6 and Figure S7, Supporting Information). Figure S6a in the Supporting Information shows the optical image of the h-BN-supported $MoTe_2$ FET on the HZO film. The corresponding transfer characteristics under different V_g sweeping ranges (±3 to ±6 V) at V_{sd} = 1 V are displayed in Figure S6b in the Supporting Information. It can be seen that the h-BN-supported device possesses a much smaller hysteresis owing to the atomically flat surface and low density of charge trapping sites on h-BN. Figure S7a in the Supporting Information shows the optical microscope image of the another control device. The control device is fabricated by the same process as that in $MoTe_2$ Fe-FET except for the substrate used here, which is based on the Si wafer with the 300 nm SiO_2. The output characteristics measured at various gate voltages in logarithmic and linear scales are displayed in Figure S7b and c in the Supporting Information, respectively, where the ohmic contact can be expected between Ti/Au electrodes and $MoTe_2$ channel due to the linear relationship between I_{sd} and V_{sd}. Figure S7d in the Supporting Information demonstrates the transfer curves under different V_{sd} conditions, which show a similar electron-dominated ambipolar transport behavior like that in the $MoTe_2$ Fe-FET. However, negligible hysteresis was observed for all measurements, demonstrating the role of ferroelectric polarizations for the non-volatile behavior.

2.2. Memory Application

Despite many previous works have employed the charge trapping mechanism for non-volatile memory applications,[33–34] however, non-ideal device performance was sometimes observed, like V_{th} instability and degradation of the reliability,[35–36] due to the limited trapping strength of the trapping states. In our work, with the help of ferroelectric polarization in the HZO film, the interfacial charge trapping effect can be strengthened, leading to stable switching behaviors. For example, the transfer characteristics of the device remain

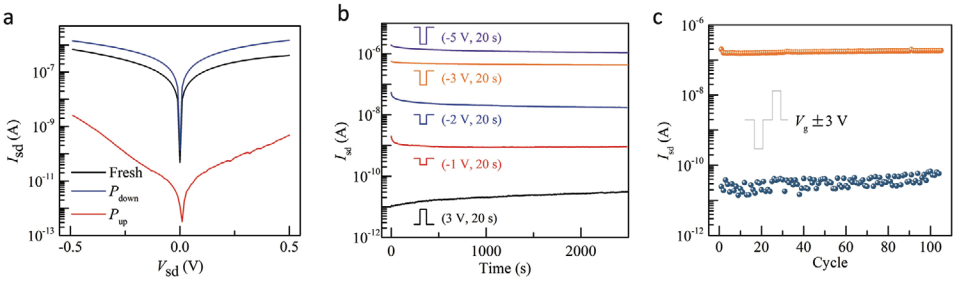

Figure 3. a) Output characteristics of the device obtained when the HZO film at Fresh, P_{down} and P_{up} states, respectively (V_g = 0 V). b) Evolution of the channel current by applying V_g pulses with different amplitudes at the fixed V_{sd} = 0.5 V. c) Endurance characteristics of the device. Cyclic (−3 V, 2 s) and (3 V, 2 s) V_g pulses were used for writing and erasing operations and the reading operation was operated at V_{ds} = 0.1 V.

stable after 100 sweeping cycles (Figure S3b, Supporting Information), making it potential for applications in reliable memory devices.

Firstly, the memory properties of the $MoTe_2$ Fe-FET device were characterized. Output characteristics of the device obtained under HZO in the Fresh, P_{down} and P_{up} states are demonstrated in **Figure 3**a. Here, P_{down} and P_{up} mean that the ferroelectric polarization is in the downward and upward directions, respectively. The low resistance state (LRS) and high resistance state (HRS) obtained in this device under different HZO polarizations exhibit a high on/off ratio up to 10^5. For the control device in Figure S7 in the Supporting Information, "P_{up}" ("P_{down}") state can also be conceptually defined as the state after applying the positive (negative) V_g to the device. The I_{sd}–V_{sd} curves (Figure S7e, Supporting Information) almost coincide with each other without memory function, which also emphasizes the role of ferroelectric polarization and interface traps in the $MoTe_2$ Fe-FET hybrid system. In addition, a broad range of intermediate resistance states can also be obtained by changing the V_g amplitudes with the stable and long-retention performance (over 2500 s), illustrating the excellent long-term storage capability (Figure 3b). Furthermore, the dynamic conductance modulation was also conducted under cyclic writing and erasing ac operations by applying voltage pulses (±3 V, 2 s) to the gate terminal and reading the channel current at V_g = 0 V and V_{sd} = 0.1 V. Reversible and reliable HRS-LRS switching behaviors with an on/off ratio ≈9×10^3 can be observed over 100 cycles, implying good endurance of the Fe-FET (Figure 3c). The memristive functionalities with multilevel and excellent retention characteristics enabled by P_r assisted charge trapping shed light on such Fe-FET device for its application in neuromorphic computing.

2.3. Synaptic Application

Emulating the basic functions of biological synapses is significant for artificial synaptic devices to construct the artificial neural network.[37–39] The biological synapses are the fundamental connecting blocks in biological neural systems, which can transmit signals among neurons. The connection strength between two neurons is known as the synaptic weight that can change over time depending on the previous history, which can give rise to many complex signal transformations in both amplitude and time domains.[40] Depending on the direction of the synaptic current (inward or outward), the membrane potential can be increased or decreased, corresponding to the evoked excitatory or inhibitory postsynaptic current (EPSC and IPSC), respectively. These behaviors can be emulated by our analog Fe-FET device via the increase or decrease of conductance induced by write and erase operations.

In our device, voltage pulses applied at the back-gate terminal (V_g) and the drain terminal (V_{sd}) are analogized as the pre- and postsynaptic spikes to trigger the postsynaptic current (PSC), where the corresponding conductance of the $MoTe_2$ channel resembles the synaptic weight (W). As demonstrated in **Figure 4**a,b, the abrupt rise and then decline of the PSC can be observed under one negative or positive presynaptic V_g pulse, corresponding to EPSC or IPSC behavior. Two kinds of plasticity, denoted as short-term plasticity (STP) and long-term plasticity (LTP), are well known in the biological system.[41–42] The STP, regarded as the physiological basis for critical computation, shows fast decay of the synaptic response on the time scale of a few seconds, while the LTP response usually lasts from minutes to hours featuring the learning and memory capability. For our device, the STP behaviors can be emulated under weak electrical stimulations, e.g., presynaptic V_g pulses with smaller amplitude or width. Then STP-to-LTP transition for the process of memory consolidation can be realized by increasing the duration time (Figure 4a and b) or the amplitude of V_g pulse (Figure 4c), where a longer retention time and stronger synaptic weight modulation ($\Delta W = \Delta PSC/PSC$) can be observed. Moreover, the STP-to-LTP transition can also be emulated by either changing the presynaptic V_g pulse number or pulse frequency, as shown in Figure 4d,e, respectively. When sequential presynaptic V_g pulses are executed to stimulate the device, the device can exhibit the cumulative potentiation behavior if the next stimulus always arrives before the full potentiation relaxation caused by the previous one, inducing the transition to LTP. In addition, pulse trains with higher frequency can also lead to a stronger synaptic response effect (Figure 4e), which successfully mimics another basic learning protocols termed as spike-rate dependent synaptic plasticity (SRDP) in neuron systems.

Paired-pulse facilitation (PPF) is a typical phenomenon in STP, which possesses the capability to transmit information contained in the temporal pattern of two consecutive actions.[43–44] In PPF, the PSC triggered by the second spike is higher than that evoked by the first one when the second spike follows the previous one subsequently. The magnitude of the PPF enhancement, represented by the PPF index $(A_2 - A_1)/A_1$,

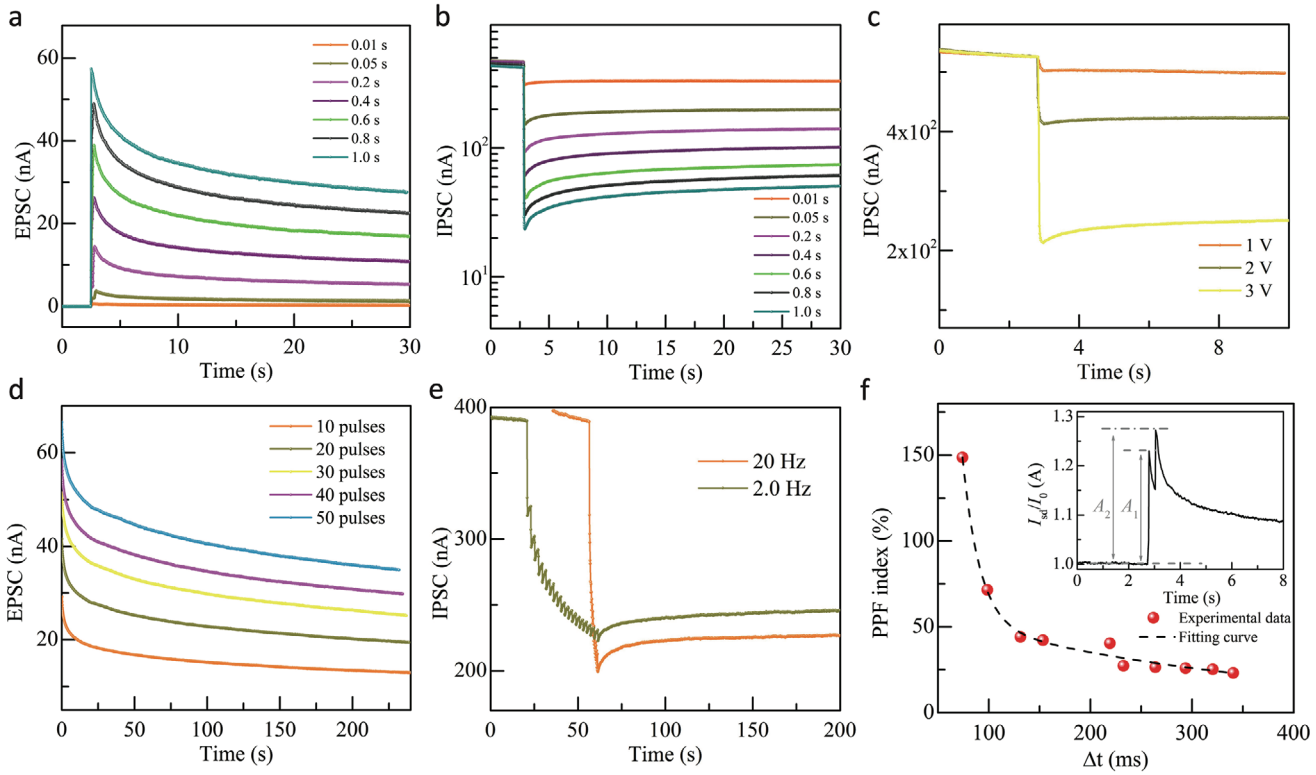

Figure 4. a) EPSC and b) IPSC of the artificial synapse triggered by one presynaptic pulse with different pulse widths. c) IPSC of the artificial synapse triggered by one presynaptic pulse with different pulse amplitudes. d) EPSC of the artificial synapse in response to multiple presynaptic pulse numbers. e) IPSC of the artificial synapse in response to 20 presynaptic pulses with different trigger frequencies. f) The plot of PPF index $((A_2–A_1)/A_1)$ with different interval times (Δt) from 50 to 350 ms. Inset: triggered EPSC by a pair of presynaptic pulses.

can be controlled by the time interval (Δt) between two spikes. Here, A_1 and A_2 are the peak values of PSC after the first and second spikes, respectively. The inset of Figure 4f demonstrates the EPSC triggered by a pair of presynaptic V_g pulses, and the obtained PPF index ratio is plotted as a function of Δt in Figure 4f. The experimental data for the PPF index decay can be fitted by a double exponential function (dotted line):

$$(A_2 - A_1)/A_1 = C_1 * \exp\left(-\frac{\Delta t}{t_1}\right) + C_2 * \exp\left(-\frac{\Delta t}{t_2}\right) \quad (1)$$

where C_1 and C_2 are the two fitting parameters, and t_1 and t_2 represent the characteristic relaxation constants. From the fitting results, the relaxation constants are extracted with the value of about 17 and 331 ms, respectively, matching well with the values in the biological synapse.

The analog-type resistive switching devices have shown the prospect to implement deep neural networks (DNNs) for neuromorphic computing.[40] According to the previous studies, analog synaptic devices should have moderate synaptic behaviors such as the G_{max}/G_{min} ratio above 10, linear conductance modulation, near-zero asymmetric ratio (AR), and a sufficient number of states for practical neuromorphic systems.[45–46]

The nonlinearity of the long-term potentiation-depression (P-D) can be represented by a parameter N to investigate the nonideal contribution from the conductance weight update, which describes the deviation from a perfectly linear conductance response. The value of N can be extracted based on the experimental data fitting through the following formulas:[46–47]

$$G(n+1) = G(n) + \Delta G_P = G(n) + A_P e^{-N_P(G(n)-G_{min})/(G_{max}-G_{min})}, \Delta G_P > 0 \quad (2)$$

$$G(n+1) = G(n) + \Delta G_D = G(n) - A_D e^{-N_D(G_{max}-G(n))/(G_{max}-G_{min})}, \Delta G_D < 0 \quad (3)$$

where $G(n)$ represents the channel conductance of the n^{th} state, N_P (N_D) is the nonlinearity of the long-term P(D) process, and G_{max} (G_{min}) represents the maximum (minimum) conductance, respectively.

Figure 5a shows the repeatable long-term P/D processes under 20 (black), 50 (red), and 80 (blue) voltage pulses with the incremental amplitude scheme. Cycle-to-cycle weight update variation (20 cycles) for the potentiation and depression can be observed in Figure 5b. Among these cycles, one representative long-term P-D process is displayed in Figure 5c, where the parameter N can be extracted with the value of $N_P = -1.24$ and $N_D = 2.4$ by fitting the data through Equations (1) and (2).

Moreover, the AR is also evaluated by the equation:

$$AR = \frac{\max\left|G_P(n) - G_D(50-n)\right|}{G_P(50) - G_D(50)}, n = 1 \text{ to } 50 \quad (4)$$

where $G_P(n)$ and $G_D(n)$ represent the device conductance values after the n^{th} excitatory or inhibitory pulses, respectively.[47] The

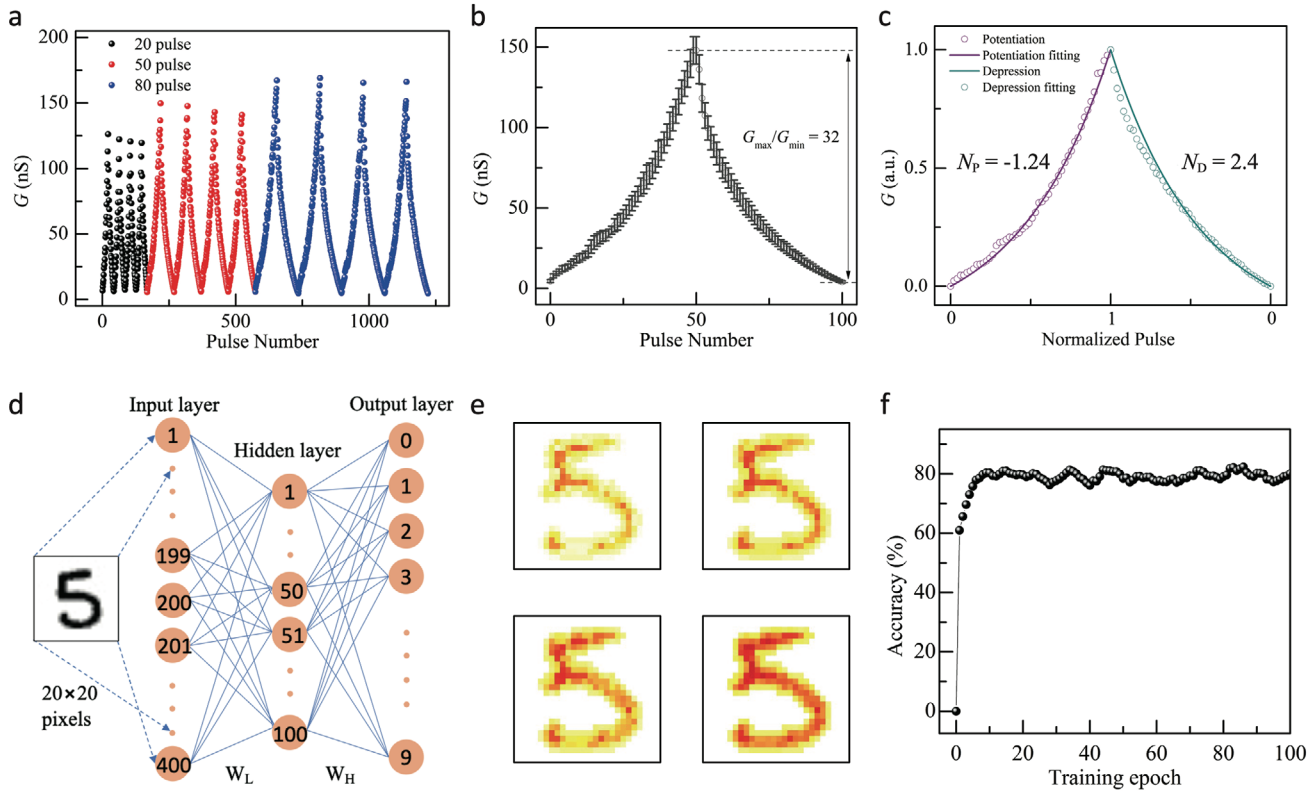

Figure 5. a) Long-term P-D properties under 20 (black), 50 (red), and 80 (blue) voltage pulses with the incremental voltage amplitude scheme. (1.5 V to 4.5 V for LTP and -1.5 V to –4.5 V for LTD). b) Cycle-to-cycle variation (20 cycles) of the potentiation and depression curves. c) Normalized long-term P-D characteristics of the device under 50 potentiation and depression pulses, with the solid lines showing the fitting curve to obtain *N*. d) Schematic diagram of an artificial neural network. e) The mapping images of the output number "5" during the training process. f) Simulated pattern recognition accuracy as a function of training epoch (0–100).

extracted *AR* value is about 0.16 (Figure S8a, Supporting Information), closing to the ideal case (*AR* = 0), further indicating the potential of the device to achieve high learning accuracy in artificial neural network simulations.

A fully connected neural network (FNN) model was constructed to perform the supervised learning of the Modified National Institute of Standards and Technology (MNIST) handwritten data set on the basis of our $MoTe_2$ Fe-FET. Figure 5d shows the schematic of the three-layer FNN consisting of the input layer (400 neurons), hidden layer (100 neurons), and output layer (10 neurons). As indicated by the dotted arrows, the handwritten image "5" consisted of 20 × 20 pixels to represent the 400 input values to the input neurons, and the 10 output neurons correspond to the recognition of digits (0–9). Each neuron node in one layer is connected with every neuron node in the adjacent layers and the connection strength (weight: *W*) between two neurons can be updated from the multiple conduction states of our synaptic devices. During each learning epoch in the simulation, 8000 patterns from the stochastically selected 60 000 images in the MNIST database were used as input data. Then, a separate set of 10 000 images were utilized to evaluate the recognition accuracy. As a result, the four representative mapping images of the output number "5" are shown in Figure 5e with the gradually increased recognition accuracy (20%, 40%, 60%, and 80%), where a much clearer shape contrast can be observed under higher recognition accuracy. Figure 5f further demonstrates the evolution of the recognition accuracy during 100 training epochs. The recognition accuracy first increases dramatically in the initial few epochs and then saturates at the high value of about 81%, which is sufficient for pattern recognition.

2.4. Reconfigurable Optoelectrical Response

Apart from the electrical characteristics, the optoelectrical properties of 2D materials are also sensitive to the interfacial states, which have also been demonstrated by extensive previous reports.[48–49] The fundamental optoelectrical properties of our $MoTe_2$ Fe-FET were investigated, showing polarization-dependent optoelectrical response, which expands the functionalities of the 2D Fe-FET device.

Figure 6a,b exhibit the output curves of the device under both dark (black curve) and illumination (λ = 638 nm, red curve) conditions measured at V_g = 0 V. A lower channel current can be observed under light illumination when the ferroelectric polarization is in the downward direction (P_{down}), corresponding to the negative photodetection, while the channel current shows the enhanced effect when the ferroelectric polarization is in the upward direction (P_{up}). Moreover,

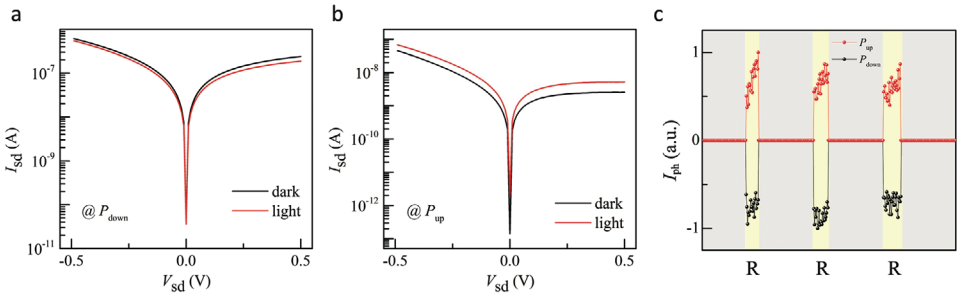

Figure 6. a) Output curves of the $MoTe_2$ Fe-FET in dark (black) and under 638 nm laser illuminations (red) when HZO is at (a) P_{down} state and b) P_{up} state, respectively. c) The dynamic logical read operation of the $MoTe_2$ Fe-FET under light illumination when HZO is at P_{up} state (red curve) and P_{down} state (black curve), $V_{sd} = 0.5$ V.

the photocurrent (I_{ph}) is calculated based on the equation: $I_{ph} = I_{light} - I_{dark}$, where I_{light} and I_{dark} are the source-drain currents under light illumination and dark condition, respectively. The normalized I_{ph} at $V_{sd} = 0.5$ V in the read operation is extracted, as displayed in Figure 6c, which shows a negative photocurrent under P_{down} state, but a positive photocurrent under the P_{up} state. A physical origin for the observed negative photocurrent is proposed as follows: when the ferroelectric polarization is pointing downwards, holes can be trapped in the surface trapping state to increase the channel current by electrostatic doping; as shown in Figure S9a in the Supporting Information, under light illumination, the photo-generated electrons will recombine with these trapped holes to lower the photocurrent in this $MoTe_2$ channel. This polarization-dependent optoelectrical response makes our $MoTe_2$ Fe-FET device promising for future non-volatile optoelectronic memory applications. Figure S9b in the Supporting Information demonstrates the schematic of a 4-cell optoelectronic memory with the integrated $MoTe_2$ Fe-FET arrays. The logical information can be electrically written into each device based on the different ferroelectric polarizations, and then optically read by monitoring the polarity of the photocurrent. For example, if a negative V_g pulse is applied to the device in the upper right corner to make HZO to the P_{down} state, the negative photocurrent under red light illumination ($\lambda = 638$ nm) can provide the logic state "0". The optoelectrical response of the control device has also been tested by the 638 nm laser (Figure S7f, Supporting Information), which can only exhibit the positive photocurrent.

3. Conclusion

In summary, abnormal clockwise hysteresis was observed in our 2D $MoTe_2$ FE-FET, which was attributed to the synergetic effect of ferroelectric polarization and charge trapping effect as corroborated through the combination of the UPS characterizations and diverse transfer characteristic measurements. Based on this mechanism, a multifunctional device was realized, including a reliable memory performance with multiple storage characteristics, and artificial synaptic functions with the STP/LTP characteristics at the single-device level, and the pattern recognition simulation at the system level. Furthermore, the ferroelectric polarization-dependent photocurrent response also makes such Fe-FET promising for future non-volatile optoelectronic memory applications. These findings demonstrate a promising strategy of using 2D materials and thin-film ferroelectric-based hybrid systems for the development of high-performance and functional devices.

4. Experimental Section

Sample Preparation and Device Fabrication: The starting Si substrate with low resistivity (10–20 mohm.cm) was first dipped into dilute HF solution to remove any native oxide present on the surface. The HZO film was then deposited on the substrate using atomic layer deposition (ALD) at 300 °C with the Picosun P300S tool through sequential deposition of HfO_2 and ZrO_2 atomic layers following a 1:1 thickness ratio. The sample was then annealed in N_2 atmosphere at 400 °C for 2h.

The 2D $MoTe_2$ flake was first mechanically exfoliated onto a polydimethylsiloxane (PDMS) film and then dry-transferred onto the HZO substrate (20 nm). Standard e-beam lithography (EBL) was utilized to define the electrodes and 5 nm/75 nm Ti/Au was then deposited through thermal evaporation. After lift-off in acetone, the as-fabricated devices were wire-bonded onto a leaded chip carrier and loaded in the customer-built high vacuum system (≈10^{-7} mbar) for electrical and optoelectrical measurements. As for the control device, the fabrication process is all the same except that the exfoliated flake was transferred onto the SiO_2 substrate (300 nm).

Material and Device Characterizations: UPS and XPS measurements of HZO film were carried out in a customer-built ultrahigh vacuum system (base pressure ≈ 10^{-10} mbar). He I (21.2 eV) and Mg Kα (1253.6 eV) were utilized as the excitation sources for UPS and XPS, respectively. PFM image and local spectroscopic measurement were carried out on a commercial scanning probe microscope (Asylum Research MFP-3D) instrument in the resonant enhanced mode. An Agilent 2912A source measure unit was utilized to perform the electrical measurements.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors acknowledge the financial support from the Natural Science Foundation of China (U2032147, 21872100, 11727902), Singapore MOE Grant MOE-T2EP50220-0001, and the Science and Engineering Research Council of A*STAR (Agency for Science, Technology and Research) Singapore under Grant No. A20G9b0135.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

artificial synapse, HfO_2-based ferroelectrics, hybrid 2D/ferroelectrics device, neuromorphic computing, non-volatile memory

Received: October 14, 2021
Revised: November 26, 2021
Published online: January 14, 2022

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