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Research Article

Two-dimensional reconfigurable electronics enabled by asymmetric floating gate

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ABSTRACT

Reconfigurable devices with customized functionalities hold great potential in addressing the scaling limits of silicon-based field-effect transistors (FETs). The conventional reconfigurable FETs are limited to the applications in logic circuits, and the commonly used multi-gate programming strategies often lead to high power consumption and device complexity. Here, we report a reconfigurable WSe_2 optoelectronic device that can function as photodiode, artificial synapse, and 2-bit memory in a single device, enabled by an asymmetric floating gate (AFG) that can continuously program the device into different homojunction modes. The lateral p–n homojunction formed in the AFG device exhibits high-performance self-powered photodetection, with a responsivity over 0.17 $A \cdot W^{-1}$ and a wide detection spectral range from violet to near-infrared region. The AFG device can also mimic synaptic features of biological synapses and achieve distinct potentiation/depression behaviors under the modulation of both drain-source bias and light illumination. Moreover, when working as a 2-bit memory via the transition between n–n^+ and p–n homojunctions, the AFG device shows four distinct conductive states with a high on/off current ratio over 10^6 and good repeatability. Combining reduced processing complexity and reconfigurable functionalities, the WSe_2 AFG devices demonstrate great potential towards high-performance photoelectric interconnected circuits.

KEYWORDS

reconfigurable device, two-dimensional (2D) materials, homojunction, photodiode, 2-bit memory, artificial synapse

1 Introduction

Silicon based field effect transistors (FETs) face the challenges in continuous down-scaling to extend Moore's Law [1, 2]. Devices based on emerging technologies or new materials are required to produce new breakthroughs in electronics [3–9]. Unlike conventional electronic devices that can only operate with unchangeable characteristics, reconfigurable devices allow the reconfiguration of every elementary unit to different functions after manufacturing or even at runtime. As demonstrated in Fig. 1(a), a complex and multi-functional electronic system can be achieved by integrating reconfigurable devices with the same configuration. These reconfigurable devices can be set to have distinctly different roles in the circuit, such as photodiode, artificial synapse, and multibit memory, to achieve different functions including signal sensing, computing, and data storage, respectively. As a result, the reconfigurable device shows great potential in realizing more complex systems with greatly simplified circuits, thereby reducing the chip area and simplifying the fabrication process.

Most previous reports focused on logic circuits based on reconfigurable FETs, which exhibit tunable polarity (n-type or p-type) of the device channel by applying different electrical signals at the programming gate terminals [10, 11]. However, constantly applying programming voltage to maintain the required functionalities of these transistors brings the issues of high power consumption, and additional programming gates lead to high device complexity [12, 13]. Therefore, it is important to investigate nonvolatile components that can maintain the programmed states after removing the voltage pulses, such as ferroelectric dielectrics and charge-trapping materials [14, 15]. This could not only eliminate the requirement of continuous electrical bias, but also enable the implementation of reconfigurable memory devices with desirable performance [16].

Layered two-dimensional (2D) materials are promising emerging materials for functional electronic devices due to their exotic electronic/optoelectronic properties [9, 17–19]. More importantly, some ambipolar 2D semiconductors with a few atomic layer thickness and sizeable bandgap possess excellent electrostatic controllability, where the carrier concentration and carrier type can be more effectively tuned by the external electric

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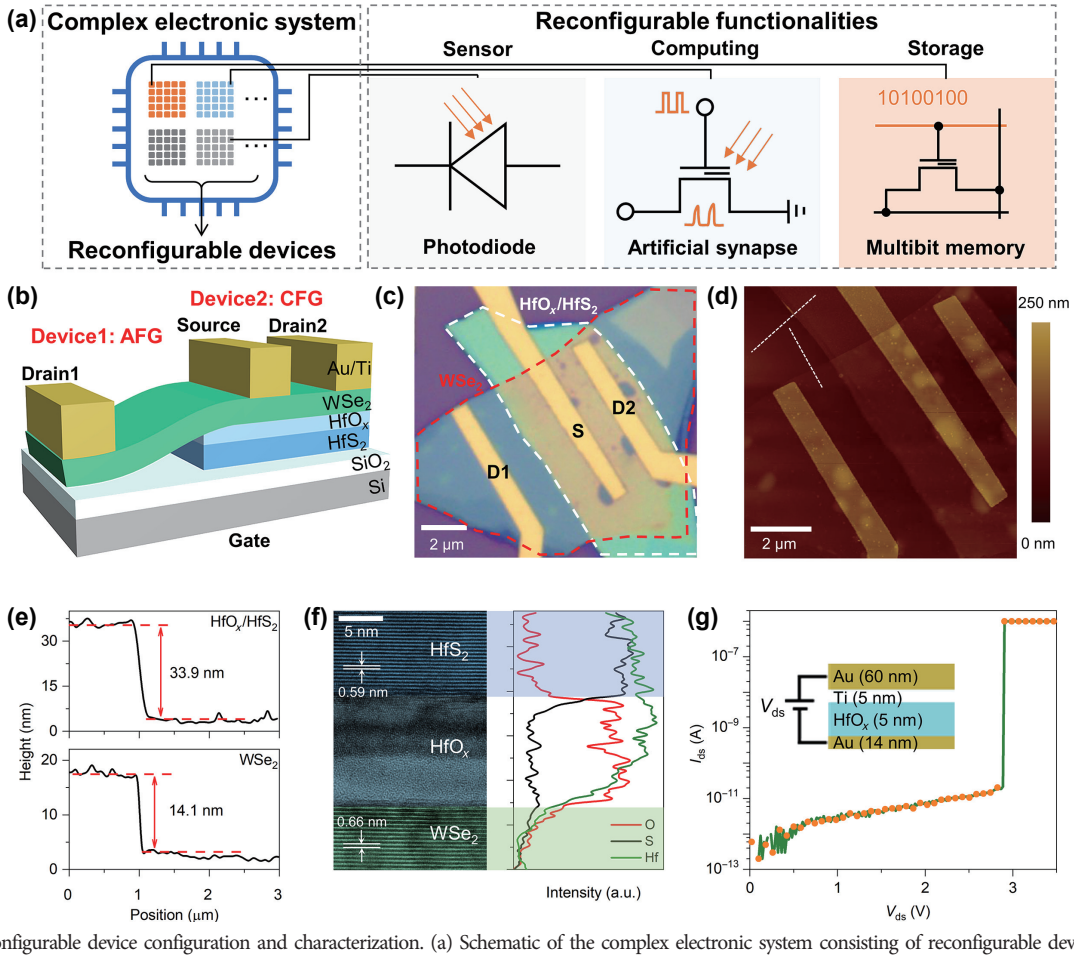

Figure 1 Reconfigurable device configuration and characterization. (a) Schematic of the complex electronic system consisting of reconfigurable devices with three examples of reconfigurable functionalities. (b) Device schematic structure of both AFG and CFG devices. (c) Optical image of the devices. Red and white lines mark the positions of WSe_2 and HfO_x/HfS_2 flakes, respectively. (d) AFM image of the corresponding devices. (e) Height profiles along the white dashed lines in (d). (f) HRTEM cross-sectional image and elemental profile of the $WSe_2/HfO_x/HfS_2$ heterostructure in the device. (g) log scale plot of the I_{ds}–V_{ds} characteristics for a MIM device with ~ 5-nm HfO_x as the tunneling dielectric. Inset: schematic of the MIM device.

field than those of three-dimensional semiconductors [17, 20]. This makes 2D semiconductors an appealing alternative for constructing electrically tunable p–n homojunctions, which are key building blocks for reconfigurable devices to demonstrate multi-functionalities, such as memory [16], logic circuit [12, 21], photovoltaic cell [14, 21–23], and photodetector [14].

In this article, we report a reconfigurable device with an asymmetric floating gate (AFG) configuration that can reversibly program the device in a nonvolatile manner. An ambipolar 2D semiconductor WSe_2 (multilayer) acts as the channel, HfS_2 and its native oxide HfO_x serve as the floating gate and the tunneling dielectric, respectively. We demonstrate that a lateral homojunction in WSe_2 can be modulated by the voltage pulses at the control gate and be further retained by the stored carriers in the floating gate. This enables the device to achieve three reconfigurable functionalities: photodiode, artificial synapse, and 2-bit memory. When operating as a nonvolatile p–n homojunction, the device exhibits excellent rectifying characteristics and high responsivity under light illumination. The reconfigurable device can also mimic synaptic features, such as short/long-term plasticity (STP/LTP). Specifically, it exhibits light-facilitated modulation of synaptic plasticity with the help of the p–n homojunction, demonstrating promising potential to improve the learning ability of artificial synapses. Moreover, the transition between p–n and n–n^+ junctions further makes the device a perfect choice as a 2-bit memory with four distinguishable resistance states.

2 Results and discussions

2.1 Structure of the floating gate devices

Figure 1(b) shows the schematic structure of both AFG device (device1 with source, drain1) and conventional floating gate (CFG) device (device2 with source, drain2). WSe_2, an ambipolar semiconductor with high carrier mobility and excellent stability is chosen as the channel material. HfS_2 and its native oxide (HfO_x) act as the floating gate and the tunneling dielectric, respectively. Note that device1 is denoted as the AFG device because only half area of the WSe_2 channel lies on the floating gate stack of HfO_x/HfS_2 and the other half lies directly on SiO_2. By contrast, in the CFG device the whole channel lies above the floating gate. The spatial asymmetry of the floating gate in the AFG device results in that only half side of the channel can be modulated by the underlying floating gate, which is the key for the AFG device to realize reconfigurable functionalities. The device preparation procedure (Fig. S1 in the Electronic Supplementary Material (ESM)) is introduced in detail in Methods. Figure 1(c) shows the optical image of the AFG and CFG devices. Red and white lines mark the positions of WSe_2 and HfO_x/HfS_2 flakes, respectively. The channel of the AFG device has a total length of ~ 3.1 μm, with ~ 1.6 μm lying on the HfO_x/HfS_2 flake and ~ 1.5 μm lying on SiO_2. To obtain the thickness of all the functional layers, the atomic force microscopy (AFM) image of the device area and height profiles along the white dashed lines are shown in Figs. 1(d) and 1(e). The height profiles indicate a ~ 33.9 nm-thick HfO_x/HfS_2 flake and a ~ 14.1 nm-thick WSe_2 flake in this device.

We have investigated the oxidation mechanism of HfS_2 and demonstrated the feasibility of applying native oxide into electronic devices in our previous work [24]. The integration of native oxide with 2D materials eliminates the usage of conventional insulators such as Al_2O_3 and hexagonal boron nitride (h-BN) fabricated by deposition or transfer methods. These methods are not compatible with 2D materials and would lead to complex fabrication process [25–27]. To get a deep insight into the oxidation process and the properties of the interfaces of the HfO_x/HfS_2 and WSe_2/HfO_x heterostructures, we investigated the cross section of the device by high-resolution transmission electron microscopy (HRTEM) and energy-dispersive X-ray spectroscopy (EDS) measurements, as shown in Fig. 1(f). We can observe atomically sharp and clean interfaces with no apparent defects or disorders at both HfO_x/HfS_2 and WSe_2/HfO_x heterostructures. WSe_2 and the unconverted HfS_2 both exhibit crystalline structure with interlayer distance of ~ 0.66 and ~ 0.59 nm, respectively, consistent with previous reports [24, 28]. However, the region between HfS_2 and WSe_2, with a thickness of ~ 14 nm, exhibits no obvious crystalline structure, indicating that HfS_2 was fully oxidized into amorphous HfO_x. The elemental compositions of the heterostructure verified by the EDS profile plot reveal a high O concentration while a low S concentration at the region sandwiched between the crystalline HfS_2 and WSe_2 and a constant Hf concentration across the whole HfO_x/HfS_2 region, consistent with the HRTEM results.

We further measured the tunneling current of a metal/insulator/metal (MIM) device configuration with HfO_x serving as the tunneling dielectric (Fig. 1(g)). The pre-breakdown current fits well with the theoretic model (Fig. S2 in the ESM) and the calculated breakdown field (~ 0.58 V·nm^{-1}) is close to those of atomic layer deposited (ALD) HfO_x (~ 0.61 V·nm^{-1}) and 2D h-BN (~ 1 V·nm^{-1}) [29, 30], indicating that the native oxide HfO_x is suitable to be used as the tunneling dielectric in the AFG devices.

2.2 Working mechanisms for the reconfigurable device

Both AFG and CFG devices work based on the tunneling of carriers through the HfO_x layer (Fig. S3 in the ESM). Due to a high conductance of WSe_2 FET at zero gate-source bias (V_g) (Fig. S4(a) in the ESM), the channel conductance is dominated by the transport of electrons. So, when electrons are depleted in the channel, we denote it as off state; when electrons return back to the channel, we denote it as on state. For the writing process (V_g = +60 V), electrons tunnel from the WSe_2 channel into the HfS_2 floating gate. The electrons are then trapped in the floating gate, serving as an efficient negative local gate to deplete the electrons in the channel, and thereby resulting in the off state. By contrast, for the erasing process (V_g = −60 V), electrons detrap from the floating gate into the channel and holes can also tunnel into the floating gate, then the holes act as an effective positive local gate to result in the on state. Although the writing and erasing processes of AFG and CFG devices are similar, the on-state and off-state characteristics are different because of the position of the floating gate.

Differences in working mechanisms for the AFG and CFG devices are illustrated in Fig. 2. For the off state of the AFG device, due to the stored electrons in the floating gate, the channel above the floating gate is turned into hole-rich region (p-type), while the channel on the left is electron-rich region (n-type) arising from the pristine electron-dominant behavior for WSe_2 FET (Fig. S4(a) in the ESM). As a result, the two regions can form a lateral p–n homojunction. In comparison, the CFG device reaches the off state simply because of the depletion of its majority carriers (electrons) under the negative local gate [31–33]. One advantage of the AFG device is that it has a much lower off-state current when drain-source bias (V_{ds}) is positive, because of the reversely biased p–n junction. However, the CFG device may suffer from a high off-state current because electrons in the floating gate will further induce holes in the WSe_2 channel (Fig. 2(d)) and WSe_2 has relatively better hole transport behavior than n-type semiconductors [34, 35]. For the on state of the AFG device, the stored holes in the floating gate turn the channel above into electron-rich region (n^+ region). It then forms a n–n^+ junction with the left unaffected region. The n–n^+ junction induces a small barrier (V_b) for electrons transporting from the right to the left. For the CFG device, the on state is obtained mainly by releasing trapped electrons back into the channel.

The transfer and output curves of the AFG and CFG devices confirm the aforementioned mechanism. As shown in Fig. 2(b), the AFG device exhibits two distinctly different transfer characteristics as V_{ds} varies from −1 V (orange and green) to +1 V (red and black), due to the AFG induced homojunctions in the device. Accordingly, the off state of the AFG device exhibits typical I–V curve of a diode, and the on-state I–V curve shows asymmetry due to the existence of V_b (Fig. 2(c)) (note that as shown in Fig. 2(a), the drain side is n-type and the source side is p-

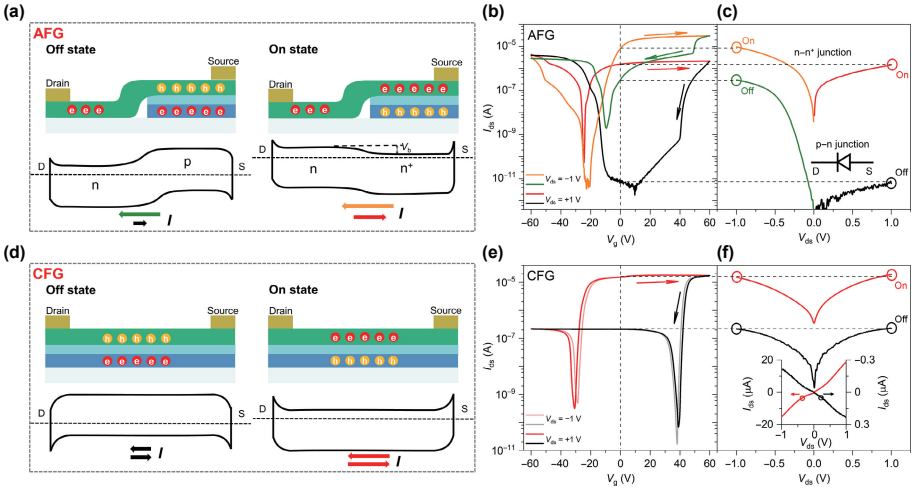

Figure 2 Comparison of the working mechanisms for the AFG and CFG devices. (a) Operation diagrams of the AFG device at off/on states and the band diagrams of the p–n/n–n$^+$ junctions. (b) Transfer characteristics of the AFG device at different V_{ds} (−1 and +1 V). (c) The on-state and off-state output curves of the AFG device. (d) Operation diagrams of the CFG device at on/off states and the corresponding band diagrams. (e) Transfer characteristics of the CFG device at different V_{ds} (−1 and +1 V). (f) The on-state and off-state output curves of the CFG device. Insert: linear scale plot.

/n$^+$-type. As a result, for the p–n junction, the diode is reversely biased when V_{ds} is positive, and forward biased when V_{ds} is negative; for the n–n$^+$ junction, the electron transport should overcome V_b when V_{ds} is positive, leading to a lower current than the negative V_{ds} case. Band diagrams of these four conditions are illustrated in Fig. S5 in the ESM). The transfer (Fig. 2(e)) and output (Fig. 2(f)) curves of the CFG device are apparently different from those of the AFG device, as the transfer curves are independent of V_{ds} polarity, and the output curves are both symmetric and nearly linearly dependent on the bias voltage. The output curves of the WSe_2 FET device (V_g = 0 V) and the as-fabricated AFG device (without any writing or erasing process) are also displayed in Fig. S4 in the ESM for comparison. The former is nearly identical with that of the on state of the CFG device, while the latter shows no apparent asymmetry and amplification effect. These results verify the effect of the AFG in modulating the channel transport behavior.

In order to test the reproducibility of the AFG device, the statistical distribution of the performance of 10 fabricated devices (at off state, p–n homojunction) in output characteristics, on current (V_{ds} = −1 V), off current (V_{ds} = +1 V), and the rectification ratio are provided in Fig. S6 in the ESM. For most of the devices, the on current, off current, and rectification ratio are centered at ~ 5 × 10^{-7} A, 10^{-11} A, and 5 × 10^4 with relatively narrow distribution, respectively. These results indicate that our devices have a good repeatability.

We also applied the AFG device configuration to another ambipolar 2D semiconductor, $MoTe_2$ (Fig. S7 in the ESM). Interestingly, we can achieve two reconfigurable p–n homojunctions with opposite direction at V_g = +20 and −20 V, due to the balanced electron- and hole-transport in the $MoTe_2$ channel. These results further prove that our AFG strategy is applicable to other ambipolar 2D semiconductors to achieve nonvolatile programmable homojunctions. We then summarized the transfer and output characteristics of WSe_2 and $MoTe_2$ devices, and also predicted the performance of devices based on hole-dominant materials, as shown in Fig. S8 in the ESM. The changes in memory windows show interesting regularity when the dominant carriers change from electrons to holes (from A to C and from D to F). The strong correlations between the transfer characteristics, the carrier type of the channel, and the polarity of V_{ds} provide us a guidance to design required reconfigurable device with customized functions.

2.3 Photodiodes

The typical diode-like I–V curve of the AFG device at the off state (Fig. 2(c)) inspires us to explore its potential in self-powered photodetection. We first evaluate the performance of the p–n homojunction by fitting the I–V curve with the Shockley diode equation including a series resistance (R_s) [36]

$$-I_{ds} = \frac{nk_BT}{eR_s} W\left[\frac{eI_0R_s}{nk_BT}\exp\left(\frac{-eV_{ds}+eI_0R_s}{nk_BT}\right)\right] - I_0 \quad (1)$$

where k_B, e, T, W, I_0, R_s, and n are the Boltzmann constant, electron charge, temperature, Lambert W function, reverse saturation current, series resistance, and ideality factor, respectively. Figure 3(a) shows both linear and log scale plot of the I–V curve. The fitted result reveals an ideality factor of 1.25 and a series resistance of 0.42 MΩ. The extracted ideality factor is closer to 1 than to 2, implying a diffusion-dominant transport in the p–n junction rather than the recombination-dominant transport via trap states within the band gap [36, 37]. It is worth noting that the highest rectification ratio ($|I_{ds}(V_{ds}$ = −1 V)/$I_{ds}(V_{ds}$ = 1 V)|) is up to 1.6 × 10^5, and the series resistance is smaller compared with previous work [38], which are beneficial to achieve highly-efficient photodetection. We have also examined the effect of programming pulse amplitude and width on the formation and the retention time of the homojunction. From Figs. S9(a) and S9(b) in the ESM, it can be concluded that a V_g pulse of ~ 50 V for 10 ms is sufficient to set the AFG device from on state to off state with a positive I_{ds} as low as 10^{-10} A. The homojunction also shows a long retention time by maintaining a high rectification ratio over 5 × 10^4 after 3,600 s (Fig. S9(c) in the ESM).

Figure 3(b) shows the energy band diagram of the photodiode operation based on the photovoltaic effect: Photogenerated electrons and holes are separated by the built-in electric field in the p–n homojunction, then accumulate at drain and source, respectively, to form the electromotive force [39]. We first explored the optoelectronic properties of the WSe_2 p–n homojunction under the illumination of a laser beam at a fixed wavelength of 515 nm but varying the power density (P_d). The I–V curves shift upwards with increasing incident laser power (P_{in},

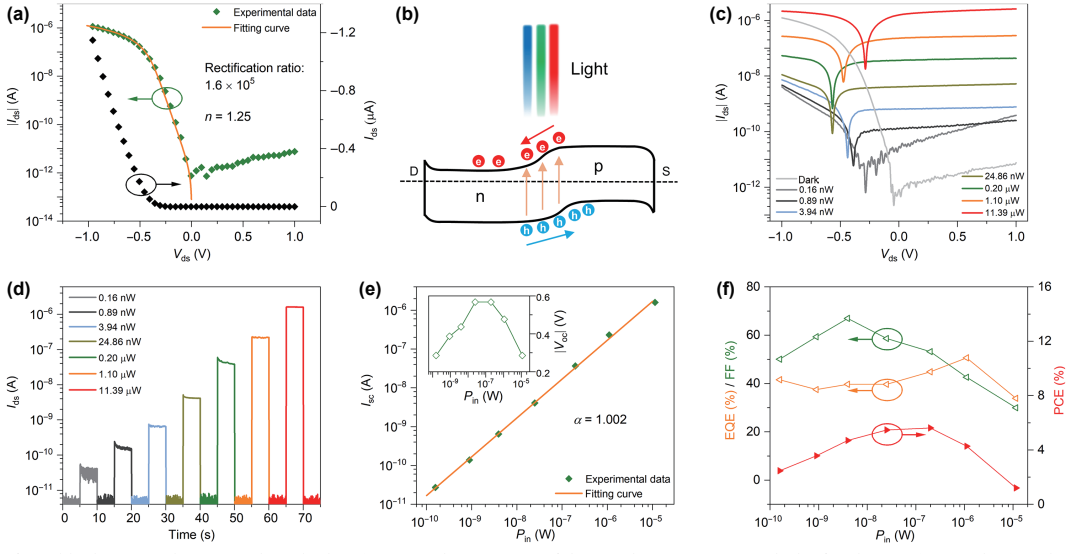

Figure 3 Reconfigurable device working as a photodiode. (a) I_{ds}–V_{ds} characteristic of the p–n homojunction with the fitted curve (orange line), indicating an ideality factor of 1.25. (b) Schematic energy band diagram of lateral WSe_2 homojunction photodiode under light illumination. (c) I_{ds}–V_{ds} curves of the p–n junction under different P_{in} (the laser wavelength is kept at 515 nm for (c)–(f)). (d) The photoresponse (with light on and off) under increasing P_{in}. (e) I_{sc} as a function of P_{in}. Inset: V_{oc} as a function of P_{in}. (f) EQE (orange symbols), FF (green symbols), and PCE (red symbols) as a function of P_{in}.

given by $P_{in} = P_d \times A$, where A should be the total area of the homojunction. For simplification, we use the value of the channel area as A. It is determined to be ~ 21.1 μm² from Fig. 1(d)), with an obvious photoresponse observed even when P_{in} is as low as 0.16 nW (Fig. 3(c)), revealing the high sensitivity. Figure 3(d) shows the photoresponse switching dynamics under increasing laser powers at V_{ds} = 0 V. The photocurrent rises suddenly with the laser switched on and quickly drops when the laser is off under every laser power. Enlarged photoresponse curve in Fig. S10(a) in the ESM further indicates good switching behaviors of the device with the rise time (τ_r) and fall time (τ_f) determined to be as short as 4.7 and 2.3 ms, respectively, where τ_r and τ_f are defined as the time for the photocurrent to rise from 10% to 90% and fall from 90% to 10% of the peak current, respectively.

The relationship between short circuit current (I_{sc}) and P_{in} extracted from Fig. 3(c) is shown in Fig. 3(e). The experimental data are fitted with equation $I_{sc} = P\alpha$, where α equals 1 for an ideal p–n junction photodiode with photocurrent depending linearly on the illumination power density. An α value of 1.002 was obtained for our device, implying that I_{sc} shows a superior linear behavior when altering P_{in} over 5 orders of magnitude from 0.16 nW to 11.39 μW. This corresponds to a linear dynamic range (LDR) of at least 97 dB according to [40]

$$\mathrm{LDR} = 20\log\frac{P_{sat}}{P_{low}} \quad (2)$$

where P_{sat} and P_{low} are the light intensity values from which the photocurrent begins to deviate from linearity. On the other hand, the open circuit voltage (V_{oc}) initially increases with the larger P_{in} but tends to be saturated to around 0.56 V and then declines with a further increase in P_{in}. The decline of V_{oc} may be attributed to the high temperature under laser illumination according to previous works about solar cells [41, 42]. However, the highest light intensity in our work is beyond 3.75×10^4 mW·cm^{-2}, which is rarely taken for the solar cell test. As a result, the mechanism for the decline of V_{oc} under ultrahigh light intensity still needs future investigation. The responsivity (R) of the photodetector follows the relationship of $R = I_{sc}/P_{in}$. Since I_{sc} depends linearly on P_{in}, R maintains an almost constant value of ~ 0.17 A·W^{-1} with different P_{in}. This value is outstanding compared with other 2D materials based homojunction devices (Table S1 in the ESM). Specific detectivity (D^*) is an indicator for the capability of detecting signals with low intensity. Assuming the dark current (I_{dark}) dominates the photodetector noise, D^* can be given by [36]

$$D^* = \frac{R\sqrt{A}}{\sqrt{2eI_{dark}}} \quad (3)$$

D^* value of ~ 6.77×10^{10} Jones irrespective to P_{in} is obtained for our WSe_2 p–n homojunction, which is close to the previously reported Si-based photodiodes ($D^* \sim 10^{12}$ Jones) [36].

Figure S10(b) in the ESM shows the linear plot of the representative I–V curve with the prominent photovoltaic effect under light illumination (515 nm, 3.94 nW), with the inset showing the generated output electrical power (P_{el}) given by $P_{el} = |I_{ds} \times V_{ds}|$ and the maximum output electrical power ($P_{el,MAX}$) point. P_{el} increases with increased P_{in}, as displayed in Fig. S10(c) in the ESM. Figure 3(f) demonstrates three important parameters for the photodiode as a function of the light power: fill factor (FF), external quantum efficiency (EQE), and power conversion efficiency (PCE). EQE is given by EQE = $Rhc/e\lambda$, where h is Planck's constant, c is the speed of light, and λ is the light wavelength; FF is expressed as FF = $P_{el,MAX}/(V_{oc} \times I_{sc})$; and PCE is defined as PCE = $P_{el,MAX}/P_{in}$. A maximum EQE of ~ 51%, FF of ~ 67%, and PCE of ~ 5.62% can be obtained for the p–n homojunction, which are superior to the values for most reported 2D p–n homojunctions [20, 36]. The decrease in PCE for weak light intensities is due to the exponential power dependence of V_{oc}, and that for strong light intensities is attributed to V_{oc} decline.

We further tested the wavelength-dependent R and EQE of the homojunction, as shown in Fig. S10(d) in the ESM. The homojunction demonstrates a wide detection spectral range from violet (405 nm) to near-infrared region (the cutoff near 1,100 nm) and maintains high R for all the wavelengths. Table S1 in the ESM lists the performance parameters of the state-of-the-art 2D materials based self-powered p–n homojunctions. Our WSe_2 AFG device has comparable or better performance compared with the state-of-the-art works in rectification ratio, ideality factor, R, D^*, and response time. These advantages together with large LDR and wide detection spectral range that were rarely demonstrated in previous works, suggesting that the AFG device is promising for self-powered weak signal photodetection.

2.4 Artificial synapse

The nonvolatility and the changeable homojunctions at on and off states enable the AFG device to possess the essential characteristics to emulate a light-facilitated artificial synapse, which is promising to realize complex learning and flexible plasticity [43–45]. Artificial synapses that mimic the biological synaptic functions are essential components for neuromorphic computing systems that are promising in addressing the challenges in traditional FET-based computing systems at the architecture level [46–50]. As shown in Fig. 4(a), the AFG device can mimic the generation of postsynaptic current (PSC) in a biological synapse [51] by the change of I_{ds} (positive/negative change corresponds to excitatory/inhibitory PSC (EPSC/IPSC)) after receiving the stimuli from the gate terminal (V_g), with the conductance of the channel reflecting the synaptic weight. The synaptic plasticity can be sorted into STP or LTP depending on whether the synaptic weight change retains for a short time or a long time [52].

High-accuracy artificial neural network (ANN) for neuromorphic computing demands linear and symmetric synaptic weight update in long-term potentiation and depression of the artificial synapses. The potentiation/depression of our AFG device was first investigated by applying 50 identical negative/positive V_g pulses (pulse amplitude: −20 V/+15 V, pulse width: 20 μs, time interval: 40 μs) under both V_{ds} = +1 and −1 V cases. As distinctly different transfer characteristics appear for V_{ds} = +1 and −1 V cases in Fig. 2(b), we expect different potentiation/depression behaviors for these two cases. As shown in Fig. 4(b), a significant increase in the mean value of PSC can be achieved in the V_{ds} = −1 V case, corresponding to a higher off-state current for the AFG device. Meanwhile, the low mean PSC for the V_{ds} = +1 V case is due to a low off-state current of the AFG device.

It is also possible for the artificial synapse to be stimulated by optical and electrical stimuli simultaneously, since we have observed a strong photoresponse when the AFG device at the off state (Fig. 3), we investigated the light-facilitated potentiation/depression behaviors for V_{ds} = +1 V case. Under constant light illumination (515 nm laser, 1 μW), both potentiation and depression processes show significantly higher PSC value (Fig. S11(f) in the ESM) accompanied with better linearity and symmetry (Fig. 4(c)). We then quantitatively analyzed the linearity and symmetry by fitting the experimental data (Fig. S12 in the ESM) with equations [53]

$$G(n+1) = G(n) + G_p = G(n) + M_P e^{-N_p \frac{G(n)-G_{min}}{G_{max}-G_{min}}}, \text{ for potentiation} \quad (4)$$

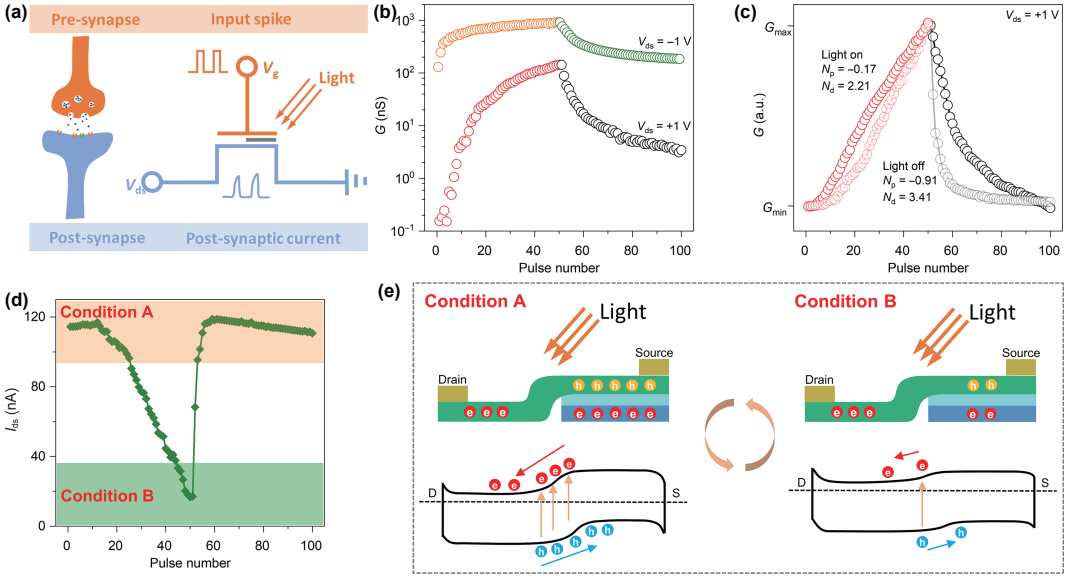

Figure 4 Reconfigurable device working as an artificial synapse. (a) Schematic of a biological synapse and an AFG device working as an artificial synapse. (b) The potentiation and depression processes measured at V_{ds} = +1 and −1 V. (c) The potentiation and depression processes measured at V_{ds} = +1 V under dark condition and light illumination. (d) Light-induced current (difference in I_{ds} measured at light-on and light-off cases) with pulse number. (e) Operation diagrams and band diagrams of the AFG device under the corresponding conditions shown in (d).

$$G(n+1) = G(n) + G_d = G(n) - M_d e^{-N_d \frac{G_{max} - G(n)}{G_{max} - G_{min}}}, \text{ for depression} \quad (5)$$

Figure S13 in the ESM shows that linearity of potentiation/depression is better when N_p and N_d values are close to 0. N_p and N_d for the light-facilitated potentiation/depression case are −0.17 and 2.21, respectively, which are much closer to 0 than those for the dark case (−0.91 and 3.41). We attribute the improved linearity to the trade-off between dark current and photo-induced current, which prevents the I_{ds} from rising too slowly and dropping too rapidly during potentiation/depression processes. It is proved by the photo-induced current during the LTP/LTD process. As shown in Figs. 4(d) and 4(e), the trapped electrons in the AFG play an important role in the whole process by tuning the built-in potential of the p–n homojunction. When the channel is at low conductance state (condition A, reversed bias of the p–n junction), the built-in potential is high, resulting in high photo-induced current. As the trapped electrons in the channel are released by voltage pulses, the built-in current is low (condition B), resulting in low photo-induce current.

We then evaluate the asymmetric ratio (A) by [54]

$$A = \frac{\max|G_p(n) - G_d(50-n)|}{G_p(50) - G_d(50)}, n = 1-50 \quad (6)$$

where A should be zero for an ideal symmetric case. The calculated A value for the light on case (0.37) is much lower than the light off case (0.66). The improved linearity and symmetry for the light-facilitated potentiation/depression reveal the important role of light in achieving high-performance synaptic weight update, making light-facilitated artificial synapse a promising candidate for high-accuracy neuromorphic computing.

We also test other basic synaptic features of the AFG device, as shown in Fig. S11 in the ESM. EPSC/IPSC was evaluated by applying single negative/positive V_g pulses with varied widths and amplitudes to simulate STP (keeping V_{ds} = +1 V), as shown in Figs. S11(a) and S11(b) in the ESM. As the pulse width increases from 0.2 to 2 ms (amplitude: −50 V), or the amplitude increases from −35 to −60 V (width: 1 ms), the peak value of EPSC is significantly enhanced and shows an increasingly longer decay time. Similarly, the IPSC value decreases significantly and experiences a longer time to return to the original state with the increased pulse width and amplitude. These results reveal that the V_g pulse polarity, amplitude, and width can efficiently modulate the synaptic potentiation and depression. Besides, Figure S11(c) in the ESM shows the EPSC induced paired pulse facilitation (PPF) characteristics of STP (keeping V_{ds} = +1 V, pulse width: 1 ms, and amplitude: −50 V). The PPF index is defined by $(I_2 - I_1)/I_1$, where I_1 and I_2 are the peak values of EPSC after the first and second pulses, respectively. The relationship between the PPF index and the time interval (Δt) between the two pulses is given by

$$\text{PPF index} = C_1 \exp\left(-\frac{\Delta t}{\tau_1}\right) + C_2 \exp\left(-\frac{\Delta t}{\tau_2}\right) \quad (7)$$

where τ_1, τ_2 are two relaxation time constants. The PPF index decreases from ~ 90% to ~ 8% with the increasing Δt, and the well fitted PPF index curve in Fig. 5(d) determines τ_1 = 5 ms and τ_2 = 119 ms, which are close to the values obtained in a reported biological synapse [55].

We then investigated the LTP behavior of the device by stimulating it with multiple pulses. Figure S11(d) in the ESM depicts the spike rating-dependent plasticity (SRDP), where the EPSC gain is proportional to pulse frequency (keeping V_{ds} = +1 V, pulse width: 1 ms, and amplitude: −50 V). For the relatively high-frequency stimulation (40 Hz), it shows a strong excitatory effect with higher EPSC peak and retained value after decay, but for the relatively low-frequency pulse input (20 Hz), the excitatory effect is weak. Spike number-dependent plasticity (SNDP), where the EPSC gain is proportional to pulse number, was also investigated (keeping V_{ds} = +1 V, pulse width: 1 ms, amplitude: −50 V, and time interval: 30 ms) in Fig. S11(e) in the ESM.

2.5 2-bit nonvolatile memory

Multi-bit memory has shown great potential in increasing the storage density and reducing the integration complexity. In principle, each β-bit memory ($\beta \geq 2$) single unit has 2^β distinguishable states. For the same storage capacity, the required device area will scale with $1/\beta$ compared with 2-state memory [56].

As aforementioned, the AFG device can be effectively reconfigured between the n–n$^+$ junction (on state) and the p–n junction (off state); both the on state and off state also possess two

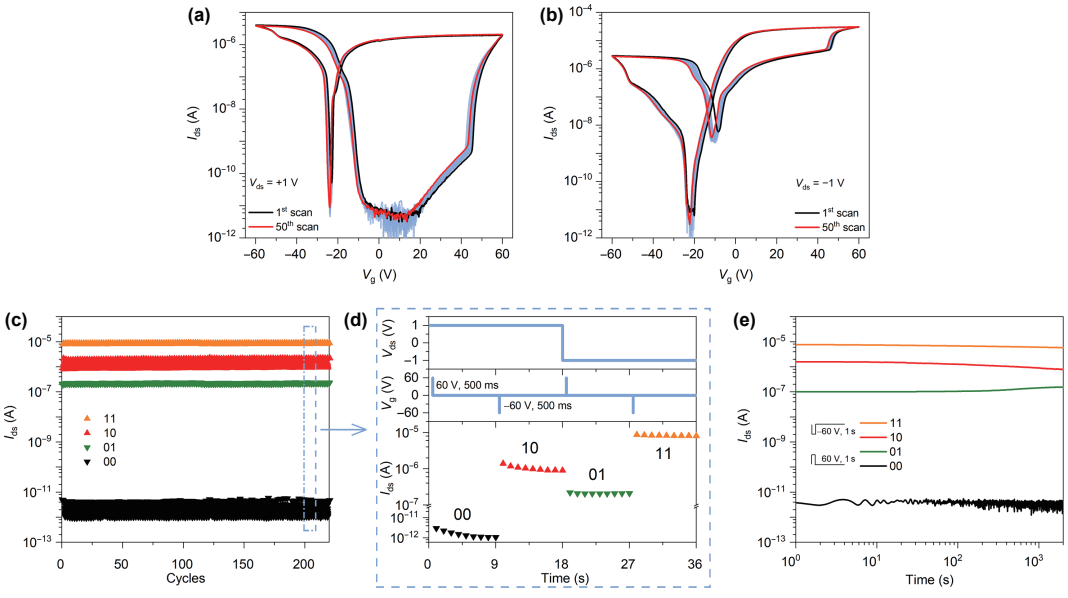

Figure 5 Reconfigurable device working as a 2-bit nonvolatile memory. (a) Transfer characteristics of the AFG device with 50 cyclic scans at V_{ds} = +1 V. (b) Transfer characteristics of the AFG device with 50 cyclic scans at V_{ds} = −1 V. (c) Endurance performance of the AFG device. (d) Four distinct current states of the AFG device under different V_g pulses and V_{ds}. (e) Retention performance of the four states (pulse width: 1 s).

different conductive states for V_{ds} = +1 and −1 V (Fig. 2(c)). Therefore, the AFG device has four distinct conductive states in total, making it a perfect choice for a 2-bit memory. By contrast, the CFG device only possesses two conductive states in total because of the symmetric output characteristics with V_{ds} (Fig. 2(f)). The four conductive states of the AFG device can also be validated from transfer characteristics shown in Fig. 2(b), with four conductive states at the reading process (V_g = 0 V) corresponding with four points in Fig. 2(c). The two transfer characteristics exhibit negligible changes in 50 repeated sweeping cycles (Figs. 5(a) and 5(b)), suggesting a good device operation stability. The two transfer characteristics in various V_g sweep ranges (V_{gmax}) were also tested, as shown in Fig. S14 in the ESM. As the sweep range increases, the shift in threshold voltage increases in these two different cases, resulting from the larger tunneling probability.

To further investigate the performance of the 2-bit memory, its dynamic characteristics were studied. The switch between the four states is shown as a function of time in Fig. 5(d). At V_{ds} = +1 V, a positive pulse (+60 V, 500 ms) was applied for setting the device to the off state (black), followed by a negative pulse (−60 V, 500 ms) to set the device to the on state (red). The same process was carried out at V_{ds} = −1 V, resulting in another two states (green for the off state, orange for the on state). As indicated in Fig. 5(d), the four different states can be denoted as 00, 01, 10, and 11 states corresponding to the black, green, red, and orange colors, respectively. The highest on/off ratio (I_{11}/I_{00}) of the 2-bit memory exceeds 10^6, and every two states are distinguishable from each other. Figure 5(c) demonstrates the reliable endurance cycles of these four states. All the states keep almost constant and the I_{11}/I_{00} ratio maintains at ~ 10^6 throughout the 220 cycles of operation. The retention time of these four states was also tested, as shown in Fig. 5(e). The data integrity was not compromised as the high I_{11}/I_{00} ratio exceeds 10^6 even after 2,000 s. Highly distinguishable states, good endurance in dynamic operation, and long retention time reveal the excellent performance of our 2-bit memory.

It should be noted that some previously reported multibit memories achieve multi-states by modulating the pulse width and amplitude to change the amount of trapped carriers in the floating gate. This method makes it hard to get stable and independent conductive states, and difficult to achieve direct and robust transition from one state to another [16, 25, 57–60]. However, in our device, multi-states are realized by switching the homojunction modes and tuning the polarity of V_{ds}, instead of changing the number of trapped carriers in the floating gate. The 00, 01, 10, and 11 states correspond to the conditions of reversed bias of the p–n junction, forward bias of the p–n junction, reversed bias of the n–n^+ junction, and forward bias of the n–n^+ junction (Fig. S5 in the ESM), respectively, which are independent with each other. Therefore, the switch between them is direct and robust.

3 Conclusions

Reconfigurable functionalities including photodiode, artificial synapse, and 2-bit memory have been realized in a single WSe_2 AFG device. The device channel can be reversibly programmed into p–n and n–n^+ homojunctions that can be retained for a long time by the trapped carriers in the AFG. By setting the AFG device to p–n homojunction, it enables high-performance self-powered photodetection, with a high LDR of 97 dB, a high responsivity over 0.17 A·W^{-1}, and a wide detection spectral range from violet to near-infrared region. The AFG device can also simulate STP and LTP behaviors of synapse, and achieve reconfigurable synaptic potentiation/depression under the modulation of both V_{ds} and light illumination. Furthermore, a 2-bit memory with four distinct conductive states and high on/off ratio over 10^6 has also been demonstrated by dynamically tuning the carrier type in the floating gate and the polarity of V_{ds}. Our study opens a route to 2D devices that can be dynamically programmed or erased, and stably operated with distinct functions, revealing the great potential of the AFG device in creating advanced sensors and processors and with simplified circuits.

4 Methods

4.1 Sample characterization

AFM images were obtained by AFM Bruker Fastscan. Focused ion beam (FIB) system (FEI Helios Nanolab 450S) was utilized to get cross-section samples. FEI Titan 80–300 TEM system operated at 200 kV was used for TEM characterization. Tecnai 20F with an Oxford EDX detector and a Gatan Imaging Filter (GIF) were used for high-angle annular dark-field scanning TEM (HAADF-STEM) and EDS analyses.

4.2 AFG device preparation

The experimental details for the preparation of HfO_x/HfS_2 and $WSe_2/HfO_x/HfS_2$ structures can be found in our previous work [24]. In brief, the mechanically exfoliated HfS_2 flakes were transferred onto a degenerately p-doped Si wafer with 300 nm oxides, followed by the O_2 plasma (power of 20 W, flow rate of 20 sccm) treatment for 10 min in a vacuum chamber (~ 10^{-5} mbar) to form a ~ 14 nm-thick HfO_x layer using Vita-Mini RIE system. To prepare the stacked structures, multilayer WSe_2 flake was then exfoliated on polydimethylsiloxane (PDMS) and sequentially transferred onto HfO_x/HfS_2 to form the vertically stacked $WSe_2/HfO_x/HfS_2$ structure. Photoresist poly(methyl methacrylate) (PMMA) was spin-coated onto the sample. The source and drain electrodes were precisely patterned on the flake using the conventional e-beam lithography technique, followed by thermal evaporation of Ti (5 nm) and Au (60 nm) as the metal contacts. After liftoff, the as-made devices were wire bonded onto chip carriers and loaded in a home-made vacuum system for *in situ* electrical measurements.

4.3 Photoelectrical and electrical characterization

The devices were characterized in a high vacuum chamber (with the chamber background pressure of ~ 10^{-7} mbar). Four laser beams (638, 515, 473, and 405 nm) and a xenon light source configured with a monochromator were used to illuminate the device. The light intensity was calibrated by THORLABS GmbH (PM 100A) power meter. The electrical measurements were conducted by using an Agilent 2912A source measure unit.

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